A QPSK MODEM FOR 2.5 MBPS DATA RATE

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By
HARINDRA RAO

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In the affectionate memory of
my elder brother,
Dr. Indrajeet Rao

CERTIFICATE

Certified that this work on "A QPSK MODEM FOR 2.5 MBPS DATA RATE" has been carried out by Harindra Rao under my supervision and that this has not been submitted elsewhere for a degree.

December, 1981

(VISHWANATH SINHA)
Assistant Professor
Electrical Engineering Department
Indian Institute of Technology
KANPUR

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December, 1981 Harindra Rao

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ABSTRACT

Efficient modem design for high speed digital communication system has been drawing considerable attention of researchers world-wide. The necessity arises because of exponential growth of data traffic. An attempt has been made in this direction by a study of QPSK modem. The theoretical studies follow hardware design and fabrication of a prototype modem which can handle data rates upto 2.5 Mbps. The performance of the modem, when compared with theoretical results, show a close resemblance between the two; the performance criterion being the usual SNR (signal-to-noise ratio) needed per bit to achieve different bit error rates (BER). An operating manual is appended.

CHAPTER 1

INTRODUCTION

The present day digital technology makes the digital communication systems more reliable at economically attractive complexity. The exponential growth of communication traffic continues to place a premium on choice of communication frequencies and channel bandwidth. As a result, there exists a need to investigate data-transmission techniques that are high in communication efficiencies, i.e., low energy per bit to noise spectral density ratio for a particular bit-error rate, and that simultaneously offer the possibilities of bandwidth conservation. The ultimate objective is to introduce bandwidth saving techniques that do not overdegrade or overcomplicate the system design problems of synchronization, data demodulation, and detection.

Various detection techniques have been studied in [1]. It is found that in binary detection the antipodal signaling, e.g., biphase shift keying (BPSK), gives the best performance compared to other binary techniques; because the distance space between the two signals is maximum. However, phase coherency is required at the receiver for coherent detection of PSK signal, which further complicates the system hardware. To overcome this difficulty, differential phase shift keying

(DPSK) is used. It is found that at small error probabilities, an increase of 1 dB in signal energy would result in DPSK performing as well as PSK [2]. The binary transmission/detection problem is readily extended to the M-ary case by considering M known signals.(i.e., $s_i(t)$, i = 1,2, ...M) for transmission/detection. The mechanization of the optimum receiver can be realized with a bank of M multipliers and finite time integrators of the type shown in Fig. 1.1, with the local input to the multiplier now being $s_i(t)$. The performance of various signal sets have been studied [1,3,4] . An orthogonal coding scheme produces error-free transmission in the unconstrained bandwidth for additive white Gaussian noise (AWGN) channel beyond a certain threshold of bit energy to noise spectral density. However this requires a complex receiver structure for detection and the time taken for decoding becomes unusually large. So block orthogonal signaling is not much useful for a practical system where the bandwidth is limited.

The requirement of high data rate per unit bandwidth led to the advent of M-ary phase shift keying (MPSK). Though this system provides a very good data rate per unit bandwidth (R/B) performance, the complexity to implement the system for large M becomes prohibitive due to phase coherency requirement at the receiver. As in the case of BPSK, here

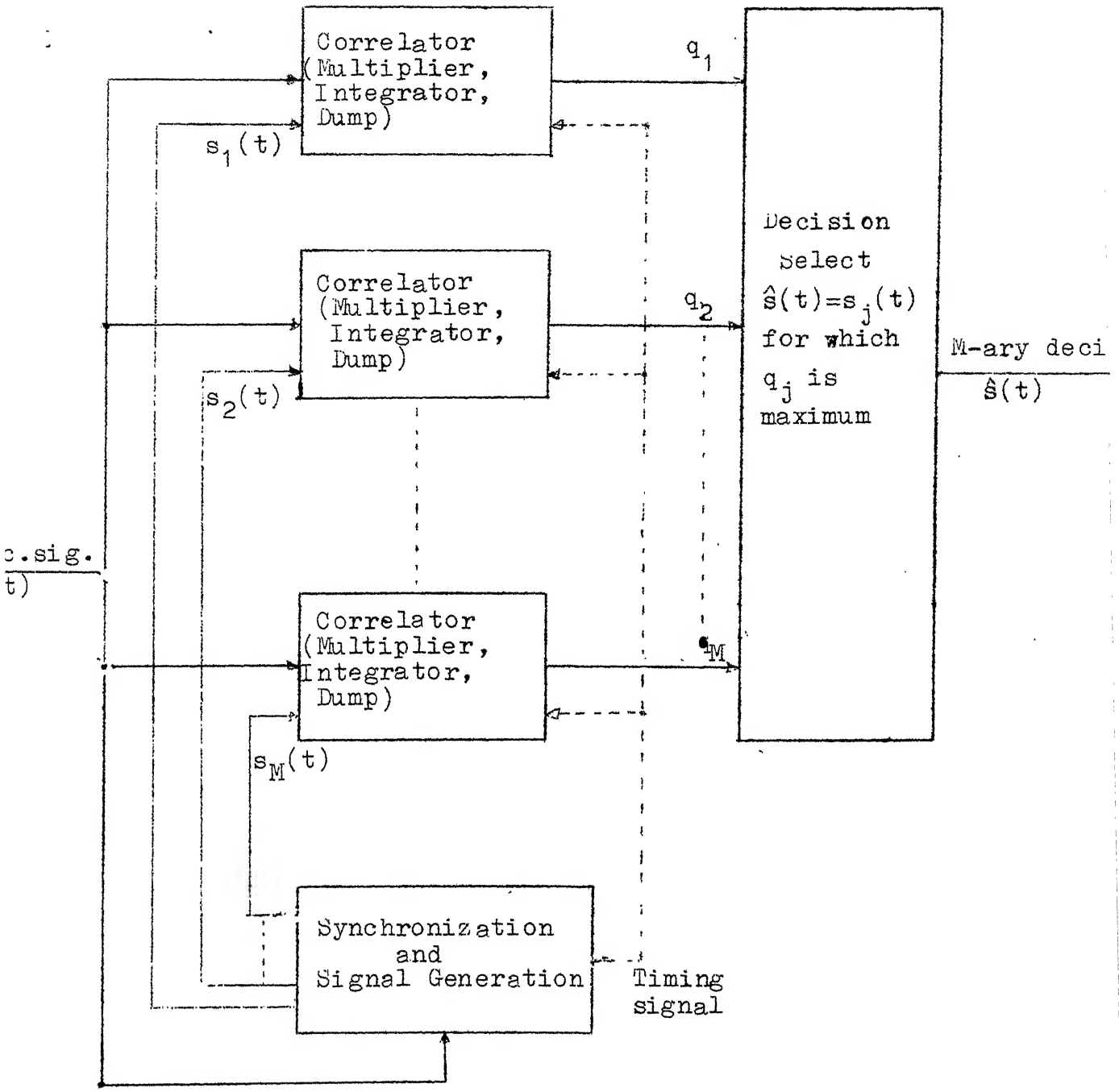


Fig. 1.1 Correlation receiver for M-ary decision problem

also the MPSK with differential detection have been tried but the probability of error performance degrades [5,6] . Hence a compromise between the complexity and data rate per unit bandwidth (R/B) has to be struck for a practical implementation of the scheme. BPSK systems have become quite common in real life applications. Experimental 8 Ø PSK system has been reported [7] . To achieve a high R/B ratio at low probability of error we have undertaken to design and fabricate a QPSK modem because of the hardware and time constraints.

With QPSK, without altering the signaling bandwidth, information rate can be doubled compared to the BPSK case. But one has to pay for this in terms of increased transmitted signal power. In fact, to keep the probability of error constant, the signal power must be doubled in the case of QPSK as compared to BPSK. In QPSK the signal set consists of two orthogonal signals and their negatives. Thus the QPSK represents a bi-orthogonal signal set. In contrast with Fig. 1.1, we note that only M/2 cross-correlators (matched filters) are required in a system that transmit M bi-orthogonal signals; this being one of the important advantages of a bio-orthogonal signal set over an orthogonal signal set. Furthermore, for the same number of signals the effective bandwidth for a bi-orthogonal set is one half of the orthogonal set [3].

Thus, we reiterate our objective, in the thesis, of going for a QPSK modem design and fabrication. We have

chosen a data handling capability (of the modem) of 2.5 Mbps from the availability of hardware components. This can easily accomodate 32 multiplexed channels each of voice grade (4 KHz) 8-bit PCM.

Theoretical analysis of QPSK signal is presented in Chapter 2. Basic problem in such a modem is the phase coherency of the carrier. Various methods to obtain the carrier and clock synchronization are discussed. The performance of QPSK for an ideal channel is given. We have chosen bit signal energy to noise spectral density ratio for achieving a certain bit - error rate (BER) as the parameters of performance.

The complete hardware realization of the modem is discussed in Chapter 3. First of all, a detailed block diagram of the modem is given. The design and function of each block is described. The complete circuit diagram is obtained for modulator and demodulator. Since we are interested in testing the performance of the modem, a channel has been simulated for experimental purposes.

In Chapter 4, the performance of the fabricated modem has been given. A comparison has been made between the theoretically available performance results and those obtained experimentally from the prototype modem.

Finally, we conclude the thesis in Chapter 5 which also outlines the scope of further studies in this area. We append the thesis with system operating manual.

CHAPTER 2

THEORETICAL ANALYSIS OF QPSK MODEM

2.1 INTRODUCTION

Our objective in this chapter is to reiterate well known theoretical details of a QPSK system. The synchronization problem for the coherent detection of QPSK has been discussed. Expression for probability of error for a QPSK system under ideal conditions has also been given.

2.2 MODULATOR CHARACTERIZATION

During a transmission interval of T seconds the transmitted signal is assumed to be characterized by the polyphase signal

$$s(t) = \sqrt{2S}\sin\left[w_c t + \frac{(2k+1)\pi}{4}\right] \qquad (2.1)$$

$k = 0,1,2,3$

w_c = Carrier frequency in rad/sec.

S = Signal power

In the QPSK case, the transmitted signal in eqn. (2.1) can be expressed in the form

$$s(t) = \sqrt{S}\,[d_1(t)\sin w_c t + d_2(t)\cos w_c t] \qquad (2.2)$$

Where $d_1(t)$ and $d_2(t)$ are digital waveforms (values ± 1) whose transitions occur at T-second intervals. Thus, for quadriphase

signaling the above equation suggests the modulator as depicted in Fig. 2.1. The four possible output phases and their d_1 d_2 digit combinations are shown in Fig. 2.2. It will be noticed that the two digit combinations are arranged in a cyclic code so that adjacent codes are separated by 90°.

Actually, in the QPSK, the input data stream (d) is converted into two parallel data streams (say d_1 and d_2) in such a fashion that two consecutive bits of input data (d) are put in the two parallel data streams and also each bit of serial data appears only once in any of the two parallel data streams. For example, if

$$d = D_1\ D_2\ D_1'\ D_2'\ D_1''\ D_2''$$

Then

$$d_1 = D_1\ D_1'\ D_1''\ \ldots\ldots\ldots$$

and

$$d_2 = D_2\ D_2'\ D_2''\ \ldots\ldots\ldots$$

Each parallel data stream modulates (BPSK) the carrier. The carriers for the two channels are in phase-quadrature having the same frequency. The outputs of the two BPSK modulators are added to get the QPSK signal. Thus, in QPSK, each symbol corresponds to two bits of information.

2.3 DEMODULATOR CHARACTERIZATION

If one assumes that the channel is a AWGN (additive white Gaussian noise), the received signal can be characterized as

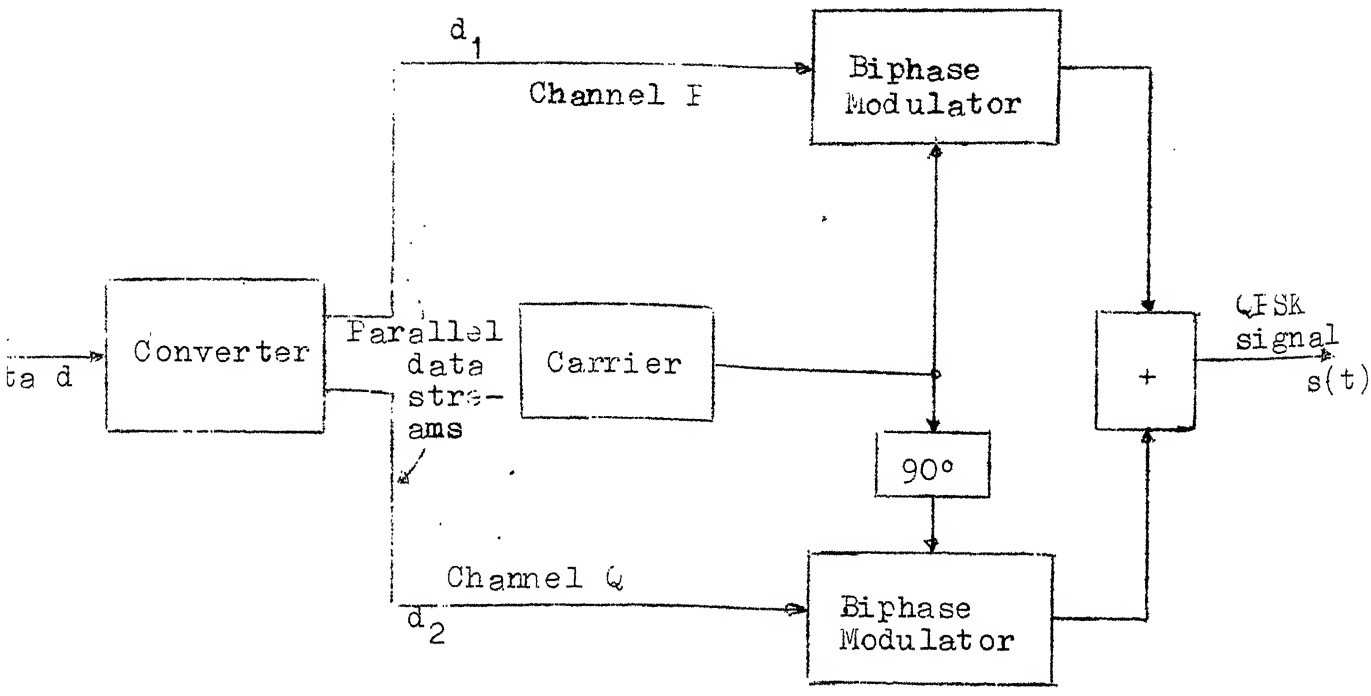


Fig. 2.1 Mechanization of a QPSK Modulator

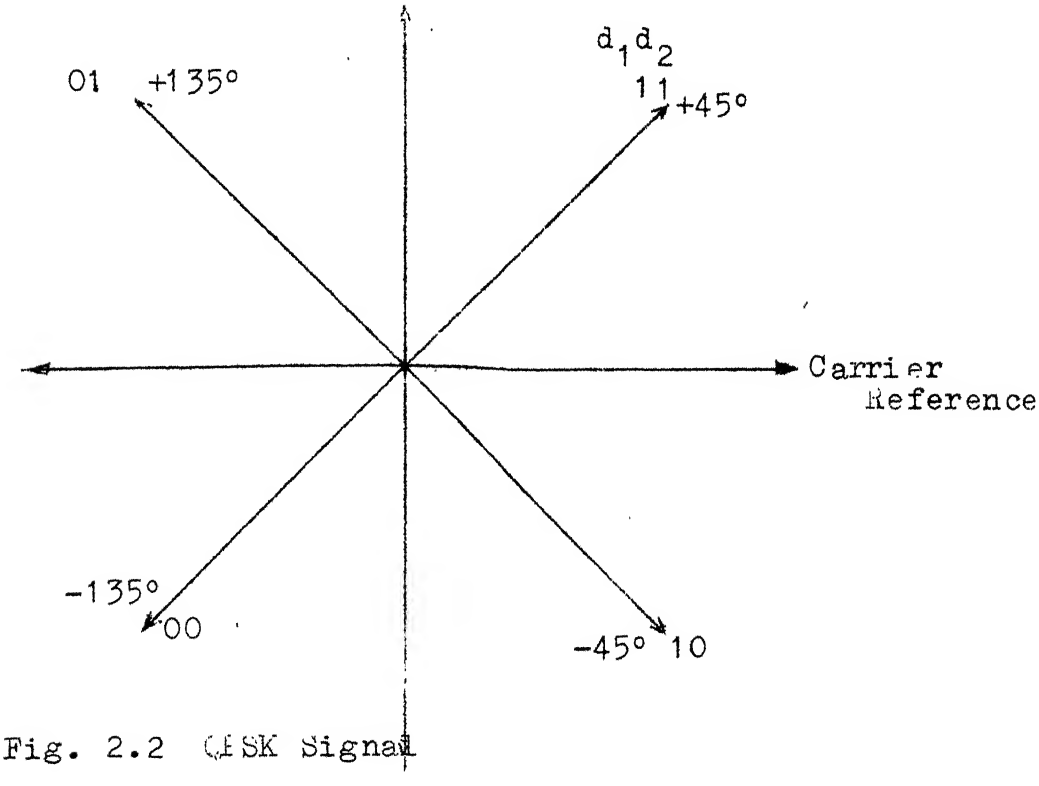


Fig. 2.2 QPSK Signal

$$y(t) = s(t) + n(t) = \sqrt{2S}\ \sin\left(w_c t + \frac{(2k+1)\pi}{4}\right) + n(t) \tag{2.3}$$

where n(t) is a sample function of the AWGN process with one sided spectral density of N_o watt/Hz. Under the assumptions of equiprobable equal energy transmitted signals, the optimum receiver (assuming perfect synchronization) is mechanized by two phase detectors followed by the decision logic and processor (Fig. 2.3) [10]. If synchronization (carrier and symbol) is to be obtained from the received signal then the carrier and symbol recovery circuitry must also be incorporated into the receiver. Generally the received signal y(t) is to be filtered by a bandpass filter Hi(p), for out of band noise rejection which gives the resulting output x(t) in the form

$$x(t) = s(t) + n_i(t) \tag{2.4}$$

$$n_i(t) = N_c(t) \cos w_c t - N_s(t) \sin w_c t \tag{2.5}$$

$$\overline{N_c^2} = \overline{N_s^2} = \overline{n_i^2} = N_o$$

where it has been assumed that W_i, the two-sided bandwidth of the BPF, $H_i(p)$, is sufficiently wide to pass the signal and $n_i(t)$ is a Gaussian noise with a narrow band expansion about the actual frequency of the input and is expressed by its inphase and quadrature components.

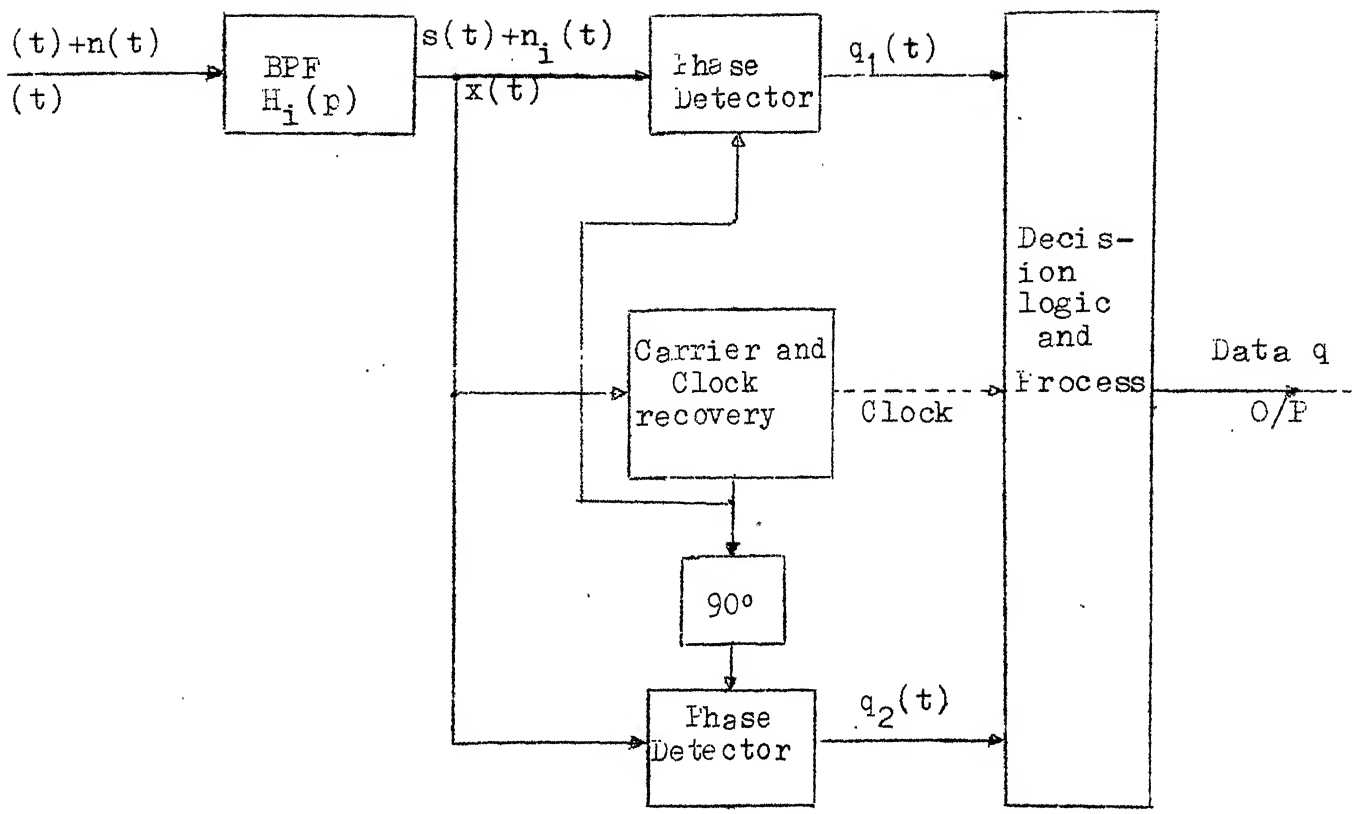


Fig. 2.3 Mechanization of a QPSK Demodulator

TABLE 2.1

Relationship between input phase & detected output

Input Phase	Transmitted Binary code d_1 d_2	q_1 0° Detection	q_2 90° Detection
+45	11	+Ve	+Ve
-45	10	+Ve	-Ve
+135	01	-Ve	+Ve
-135	00	-Ve	-Ve

The Table 2.1 shows the relationship between the input phases, their digital assignments, and the polarity of detected output without any error in the absence of noise.

2.3.1 Carrier Recovery

Since perfect carrier (reference) recovery is essential for error free detection, the performance of the demodulator circuit depends primarily on quality of the recovery circuit for the reference signal. Since highly stable oscillators are available, it is possible to establish a phase reference in the receiver which will track the varying phase and help in detecting the digital phase modulated signals. The reconstruction of a carrier for a polyphase signal can be accomplished in many ways; however, if the modulation scheme is to be successfully implemented one must provide an efficient and accurate method for establishing reference coherence in the receiver. This statement implies that the receiver must be capable of tracking the carrier phase at all times.

The simplest carrier synchronization systems that satisfy this requirement consists of the generalization of the suppressed-carrier tracking loops presented and analyzed in [11]- [13] to M phases. The reconstruction of a carrier reference from a polyphase (MPSK) signal can be accomplished by Mth power loop (the generalized squaring loop), the

generalized Costas (I-Q) loop, modulation wipeoff techniques employing decision directed methods, etc. [8,10] .

We shall not discuss the mathematical details of various carrier synchronization techniques, as these are readily available in [10] . From a practical point of view, the M-phase Costas loop suffers for large M in that the amount of equipment needed for implementation becomes prohibitively complex. Other practical considerations regarding the use of one circuit over the other follow the comments made in the above references. One final point is that the probability density function for either M-phase tracking loop exhibits M-1 equally probable ambiguities in the interval $(0, 2\pi)$ and hence practical implementation of these circuits in combination with a data demodulator would imply providing a means for resolving these ambiguities, which becomes increasingly difficult for larger M. There are various methods of resolving the phase ambiguities in practical systems [14] . For example, one can employ differential encoding of the signals or search for a known synchronization pattern within the data stream. In any case, a certain amount of signal energy must be expended to accomplish ambiguity resolution.

In our case, M is equal to four which is not too large for implementation of 4 phase Costas loop. Since performance

of Costas loop under various impairments of received signal is better than generalized squaring loop, we have chosen to go for Costas loop for carrier recovery in our modem (Fig. 2.4). We discuss the resolution of phase ambiguity in Chapter 3.

2.3.2 Clock Recovery

The clock is also needed at the demodulator for further processing so that one can recover the exact transmitted data. Transmitted signal does not contain discrete spectral component of the clock. No linear network can recover a reference that does not exist. The clock is recovered from envelope variation of the received signal or by the non-linear operation on the demodulated baseband waveforms [15]. In contrast to the limited number of carrier regenerators, there are many possible clock-generator circuits. We discuss here the rectifiers, which essentially recover timing information from envelope variations that accompany bandwidth-limited signals. A rectifier can provide excellent performance on a band-limited signal; other circuits might be more suitable for wide band signals with constant envelopes.

Square law and absolute value ("linear") rectifiers were investigated in depth. Practical rectifier circuits

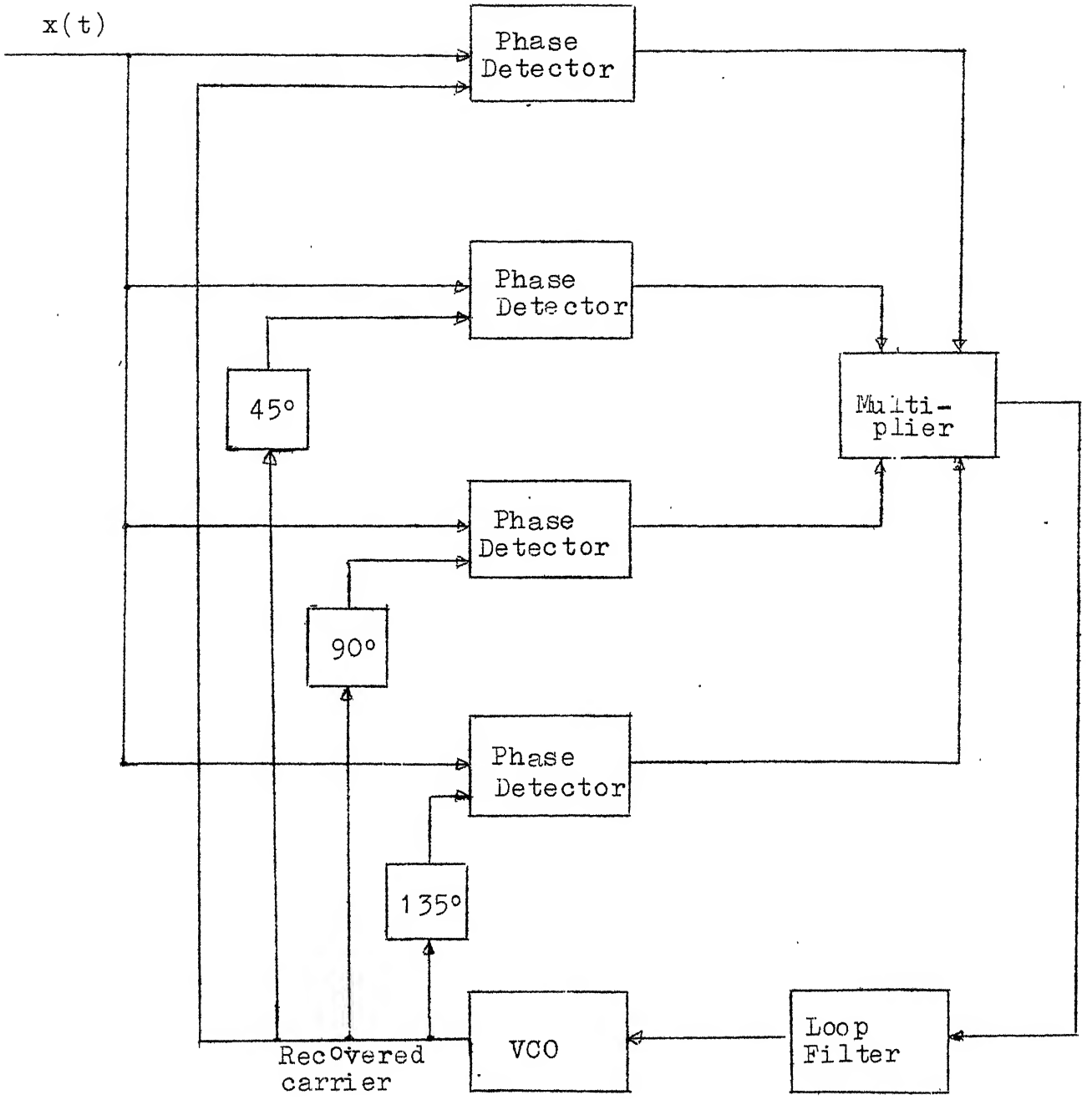
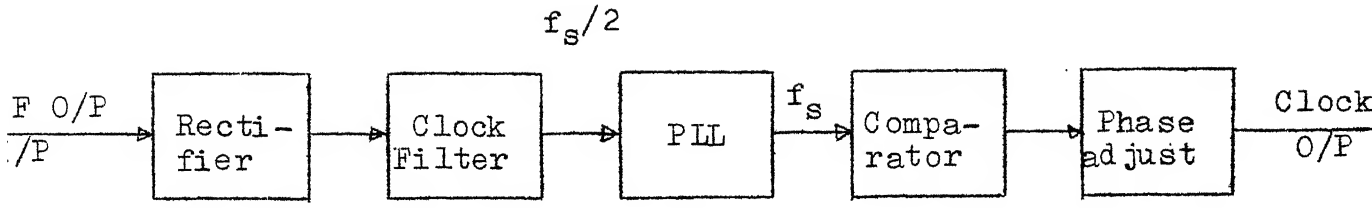


Fig. 2.4 4 Phase Costas (I-Q) Loop

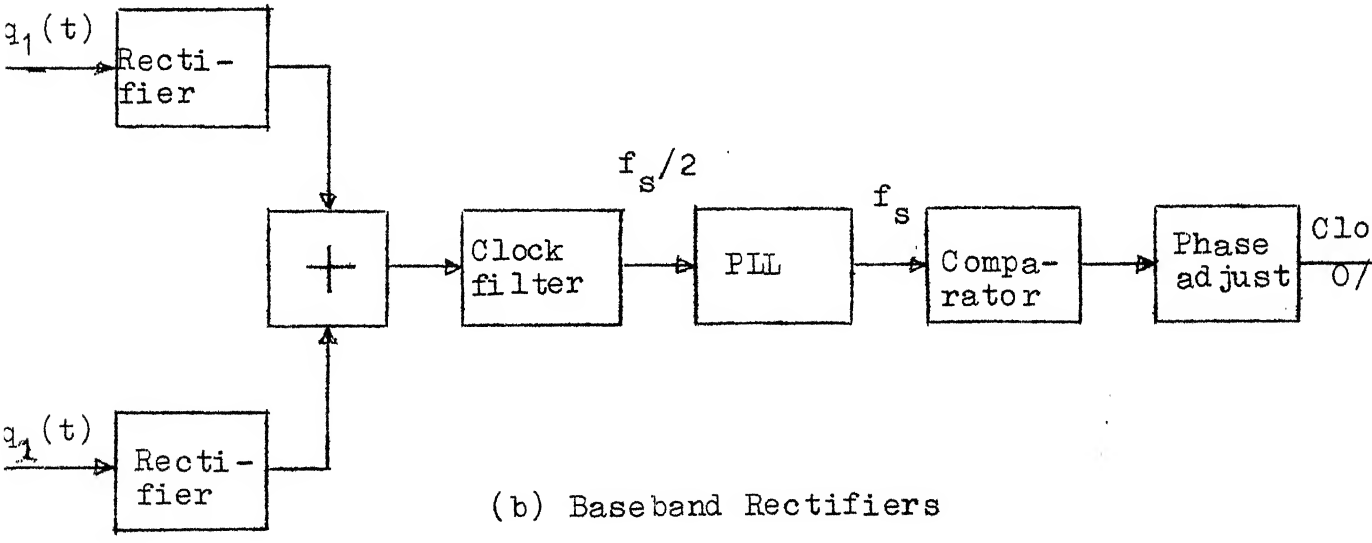
probably have characteristics that lie between the ideal square law and absolute value extremes. Rectifiers can be used at the IF output (in our case there is no RF so at the input of the demodulator) or at baseband (Fig. 2.5). All IF rectifiers supply a regenerated clock that is independent of carrier phase. The absolute value rectifier provides a clock with less noise jitter than does its square law counterpart [15] . The clock filter is a sharply tuned filter. Amplitude phase and noise transients of typical filters were examined in detail. It is found that a single tuned filter will serve our purpose. A single tuned filter may allow certain cycle-skip events that are much rarer with a high order filter. Cycle skips are extremely destructive if they occur in the bit synchronizer. Hence, a phase-locked loop (PLL) has been employed at the output of clock filter. The PLL takes care of cycle-skips. The characteristic of the PLL is such that once locked it takes a long time to be unlocked. One thing should be clear that at the output of tuned filter, the recovered clock frequency will be half of the actual clock employed at transmitter. So with the help of the PLL the required clock frequency is synthesized.

2.3.3 Decision Logic and Processor

The decision rule is such that, if demodulated signal $q_1(t)$ or $q_2(t)$ is positive, it correspond to 1 (binary) and



(a) IF Rectifier



(b) Baseband Rectifiers

Fig. 2.5 Clock recovery rectifiers.

it is 0 for negative values of signal. Thus at the demodulator there are two parallel data streams and they have to be converted into an appropriate serial data stream. The conversion is in such a fashion that any two consecutive bits of a parallel data stream are not adjacent in the serial data stream and also one bit will appear only once in the serial data. For example, if

$$q_1 = Q_1 \; Q_1' \; Q_1''$$

$$q_2 = Q_2 \; Q_2' \; Q_2''$$

then

$$q = Q_1 \; Q_2 \; Q_1' \; Q_2' \; Q_1'' \; Q_2''$$

This serial data (q) will be the output of the modem.

2.4 PERFORMANCE OF QPSK

Early work on performance of digital communication systems employing polyphase signals was developed by Cahn [6,16,19] . Arthurs and Dym [9] presented a geometric interpretation of three basic data transmission systems.

The probability of error of MPSK for large M under ideal conditions has been given in [1].

$$P_e(m) \simeq \text{erfc} \left(\sqrt{\gamma} \sin \frac{\pi}{M}\right) \qquad (2.6)$$

where γ is symbol SNR.

The probability of error of QPSK under ideal conditions, (i.e., the channel is an AWGN, there is no ISI and there is no delay distortion introduced by the channel), is given [3]

$$P_e(4) = \text{erfc}\ \sqrt{\gamma_b} - \frac{1}{4}\ \text{erfc}^2\ \sqrt{\gamma_b} \qquad (2.7)$$

where P_e = Symbol error rate

γ_b = Bit SNR

$$\gamma_b = \gamma/\log_2 M .$$

From Eqn. (2.6) it is evident that for fixed information rate operation, the SNR per bit and hence signal power S must be increased as $M^2/\log_2 M$ to maintain the constant symbol error rate with increasing M. However, the required signaling bandwidth reduces as $1/\log_2 M$. If we have fixed signaling bandwidth operation, maintaining the same symbol error probability with increasing M requires that SNR per bit (γ_b) be increased as $M^2/\log_2 M$ while the information rate increases as $\log_2 M$. However, to compensate for the increased information rate, the transmitted power S must be increased as M^2 [18] . Thus it is clear that coherent QPSK provides the same error probability performance as biphase PSK (BPSK) and requires only the half the bandwidth. So there is 3 db improvement in bandwidth at the cost of 3 db degradation in transmitted power. The relationship between bit error rate and symbol error rate is given [3].

$$P_{eb}(M) = P_e(M)/\log_2 M \qquad (2.8)$$

where P_{eb} = Bit error rate (BER) for MPSK

$$P_{eb}(4) = \frac{1}{2}\left[\operatorname{erfc}\sqrt{\gamma_b} - \frac{1}{4}\operatorname{erfc}^2\sqrt{\gamma_b}\right] \qquad (2.9)$$

The theoretical (calculated) and experimental values of BER for the fabricated modem for different values of Bit SNR have been compared in Fig. 4.1.

In an ideal case a bandwidth f_s is sufficient to send signal by BPSK at a rate f_s bits per second without intersymbol interference (ISI). This allows for upper and lower side bands with widths $\frac{fs}{2}$. In QPSK, it is ideally possible to send a choice of one out of four phases in a time interval equal to the reciprocal of bandwidth B. Each choice represent two bits of information and hence the bit rate is 2B. So for QPSK the bandwidth B will be [17].

$$B = \frac{fs}{2} \qquad (2.10)$$

CHAPTER 3

HARDWARE DESIGN AND REALIZATION

3.1 INTRODUCTION

In this chapter, we discuss hardware design for the QPSK modem. A hardware design tries to achieve theoretical values within certain tolerance limits. These are dictated because of component considerations, and availability of components etc. The complete system model of the modulator and the demodulator has been shown in Figs. 3.1 and 3.2 respectively. The specifications for the job at hand are:

MODULATOR:

INPUT: DATA TO BE TRANSMITTED, WITH THE CLOCK SEPARATELY AVAILABLE
(INPUT TTL COMPATIBLE)

INPUT DATA RATE = CLOCK FREQ. = f_s = 2.5 MBPS

OUTPUT : MODULATED SINE WAVE CARRIER AT FREQ. 10 MHz

DEMODULATOR:

INPUT: RECEIVED SIGNAL POSSIBLY CORRUPTED BY CHANNEL

BANDWIDTH OF BPF= 2.53 MHz

DESIRED OUTPUT: DETECTED DATA (TTL COMPATIBLE)

3.2 DESIGN OF MODULATOR

Input to the modulator is a serial binary data at 2.5 Mbps. This may, in a practical situation, come from a

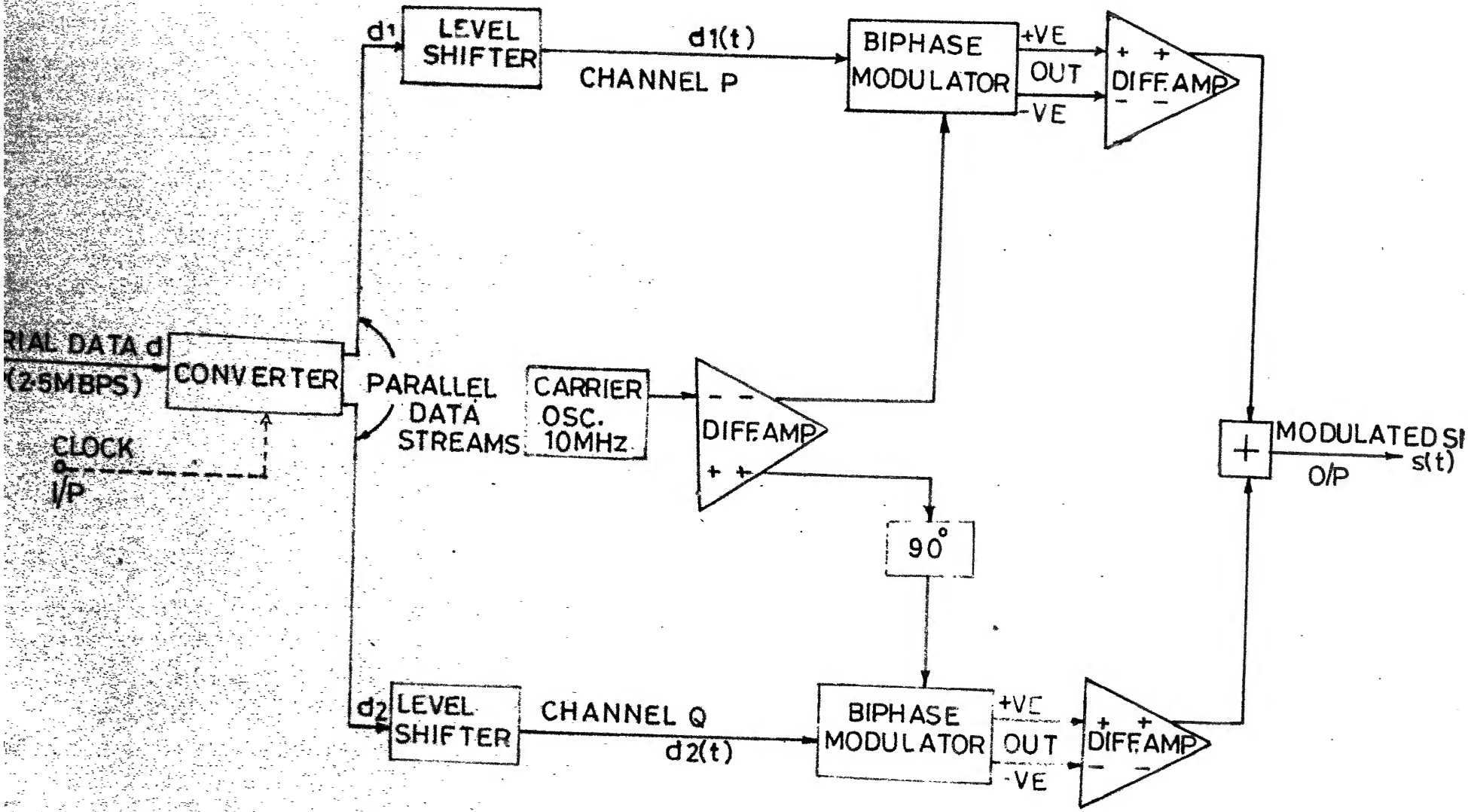


Fig. 3.1 QPSK Modulator

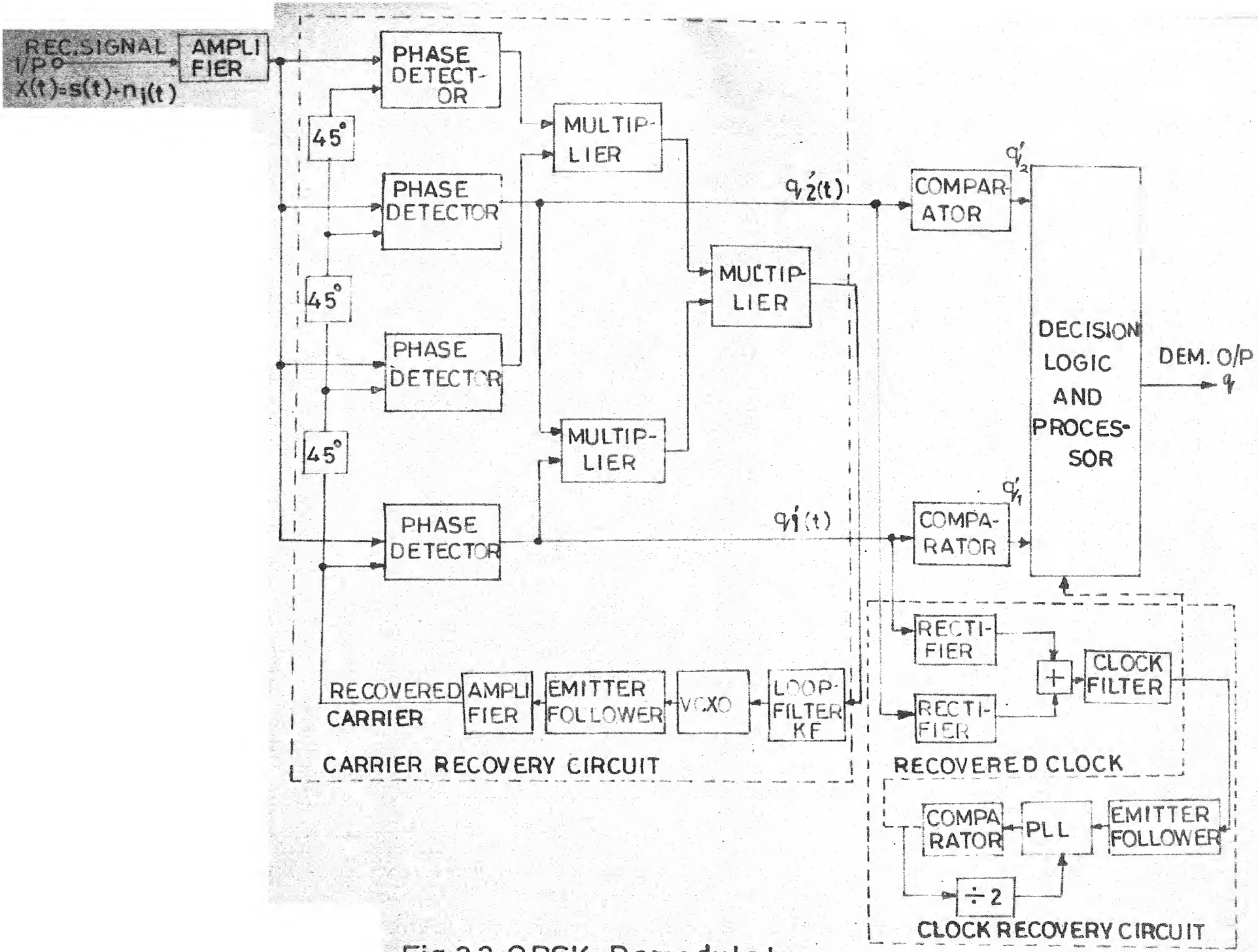
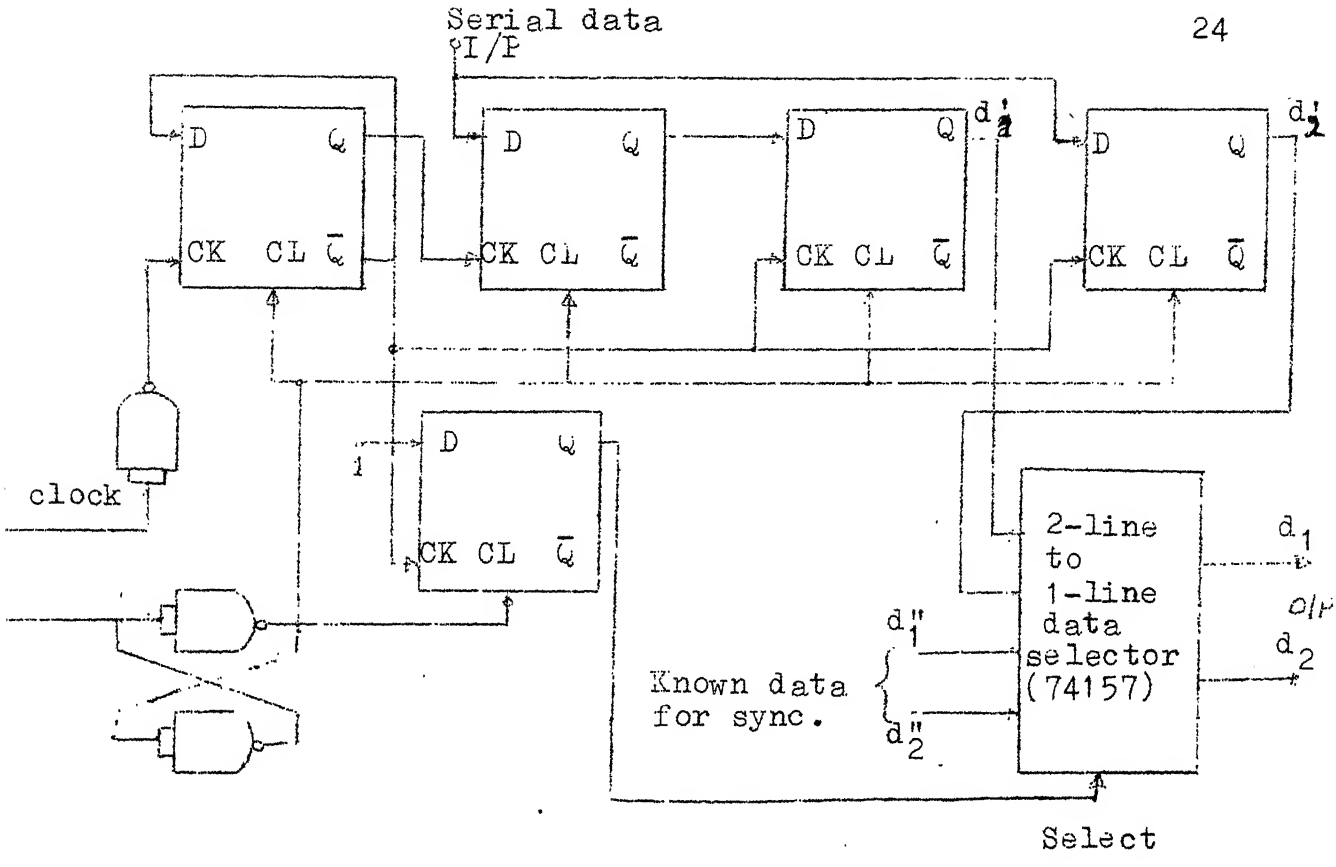


Fig. 3.2 QPSK Demodulator.

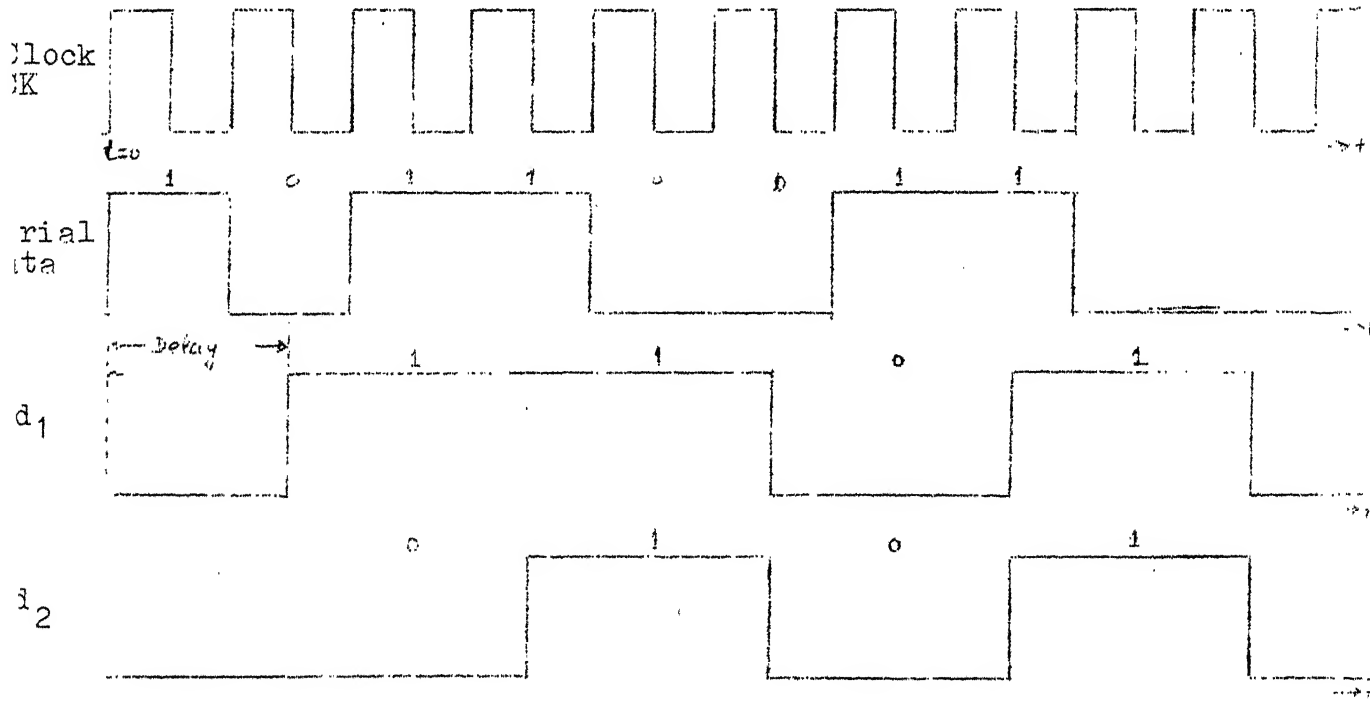
multiplexer of 32 voice grade 8-bit, PCM channels appended with suitable control protocols. The circuit clock filter followed by the phase-locked loop (PLL) has been designed for the 2.5 Mbps rate. The system will also work for lower rates but thefilter and the PLL have to be suitably modified. The modulator takes this serial binary data as its input and produces QPSK signal with the subcarrier frequency of 10 MHz. The modulator block diagram given in Fig. 3.1 is self explanatory, however we shall discuss individual blocks in detail from design considerations.

3.2.1 Converter

The serial input data applied to the modulator is converted into two parallel data streams in a particular fashion as discussed in Section 2.2. Obviously, the data rate in either channel will be half of the input data rate. We assume that in the serial data, coming from the source, transitions occur at the leading edge of the clock. In the laboratory this is readily available from a data generator. Since the transition in both the parallel channels, if any, must occur at the same instants, we shall delay the upper channel P by a bit with the help of a flip-flop. Thus, we achieve the perfect synchronization of the two channels. The complete circuit diagram of the converter is shown in Fig. 3.3(a together with an input and corresponding output waveforms



(a) Circuit Diagram



(b) Input and Output Waveforms

Fig. 3.3 Converter

(Fig. 3.3(b)). The 2-line to 1-line data selector (used in converter) enables us to send a known data pattern to resolve the phase ambiguities of the recovered carrier, before starting the transmission of actual data. All the flip-flops must be cleared before starting the operation. The following is the state of operation of the converter.

When CLR = 1 $d_1 = d_1''$ $d_2 = d_2''$

CLR = 0 $d_1 = d_1'$ $d_2 = d_2'$

where d_1'' and d_2'' are known data streams (to resolve phase ambiguity) and d_1' and d_2' correspond to serial data to be transmitted.

3.2.2 Level Shifter

Since the biphase modulator requires the amplitude of the modulating signal around +.5V and -.5V corresponding to 1 and 0 of the data respectively, the level of the digital (TTL output) signal is shifted by the circuit of Fig. 3.4.

3.2.3 Carrier Oscillator [20]

We need a very stable oscillator for carrier generation. The 10 MHz sine wave carrier is obtained by a Pierce crystal oscillator as shown in Fig. 3.5. Some typical performance characteristics of the oscillator are given below.

a. Crystal : 10 MHz

b. Output : .9V peak-to-peak for $R_L = 430\Omega$

c. Permissible load: $100\Omega \leq R_L \leq \infty$

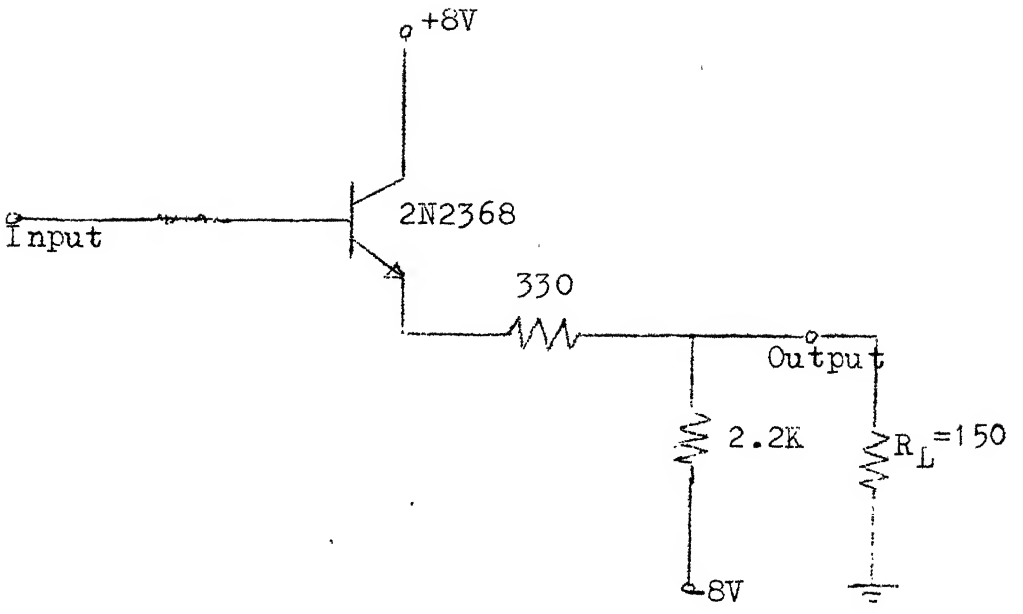


Fig. 3.4 Level Shifter

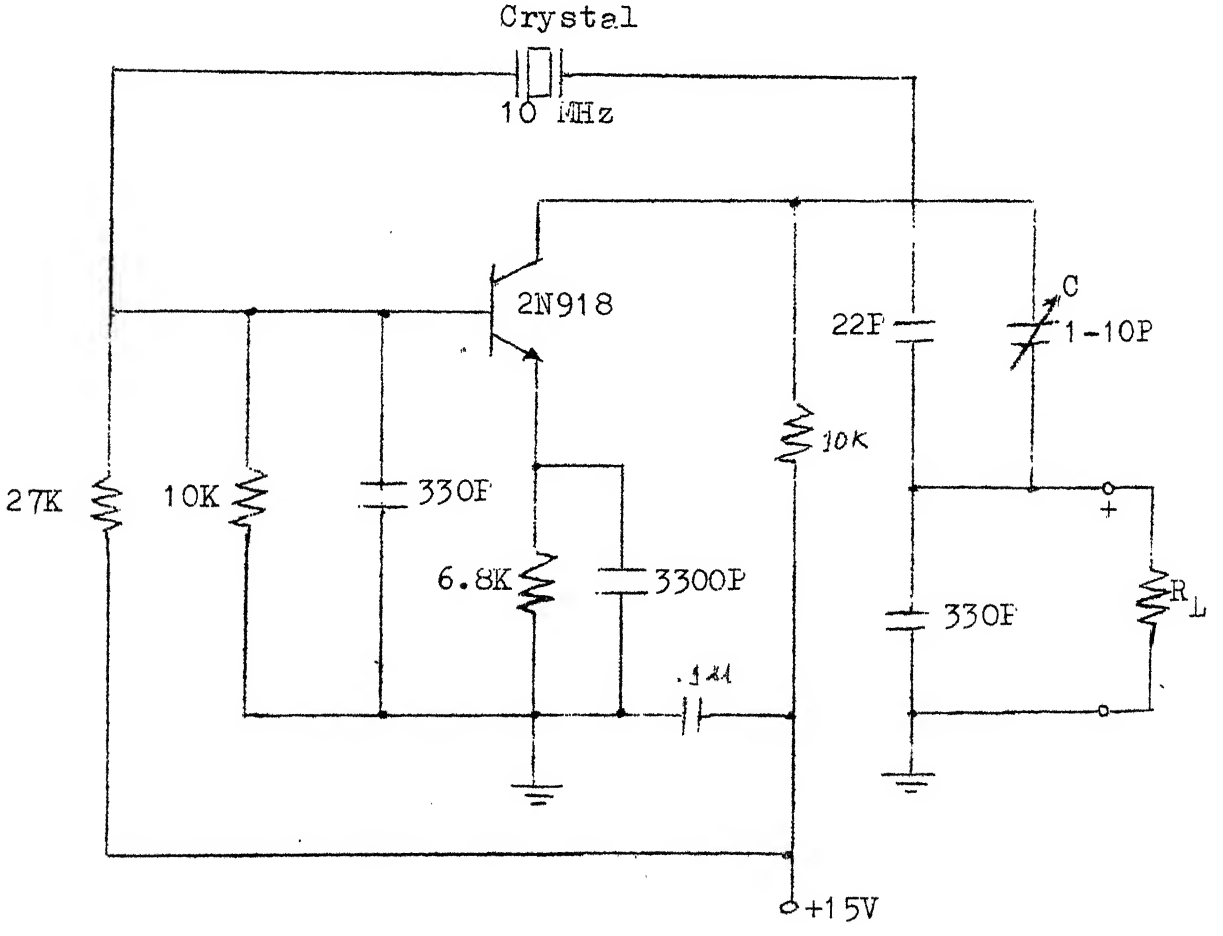


Fig. 3.5 10 MHz Pierce Oscillator

The circuit will oscillate with any standard crystal but the particular oscillating frequency is obtained by suitable adjustment of C .

3.2.4 Differential Amplifier

For carrier or modulated signal amplification/addition, the video differential amplifier LM733 has been used. It has differential input and differential output configuration. However, it can be used in any mode depending upon the requirement. The gain can be adjusted between 10 to 400. The input and output resistances are around 250KΩ and 20Ω respectively. The maximum output current is 10 mA. A typical differential amplifier is shown in Fig. 3.6.

3.2.5 Phase Shifter

The phase shifter can be realized with the help of a high slew rate operational amplifier. But due to nonavailability of the component, the configuration shown in Fig. 3.7 has been used. It consists of an RC section, an emitter follower, and an amplifier. The phase shift between input and output is adjusted to be 45°. To increase the phase shift, similar sections have been cascaded. The phase shift (θ) is given as

$$\theta = - \tan^{-1} wRC \qquad (3.1)$$

where $C = C_1$ + Input capacitance of the emitter follower.

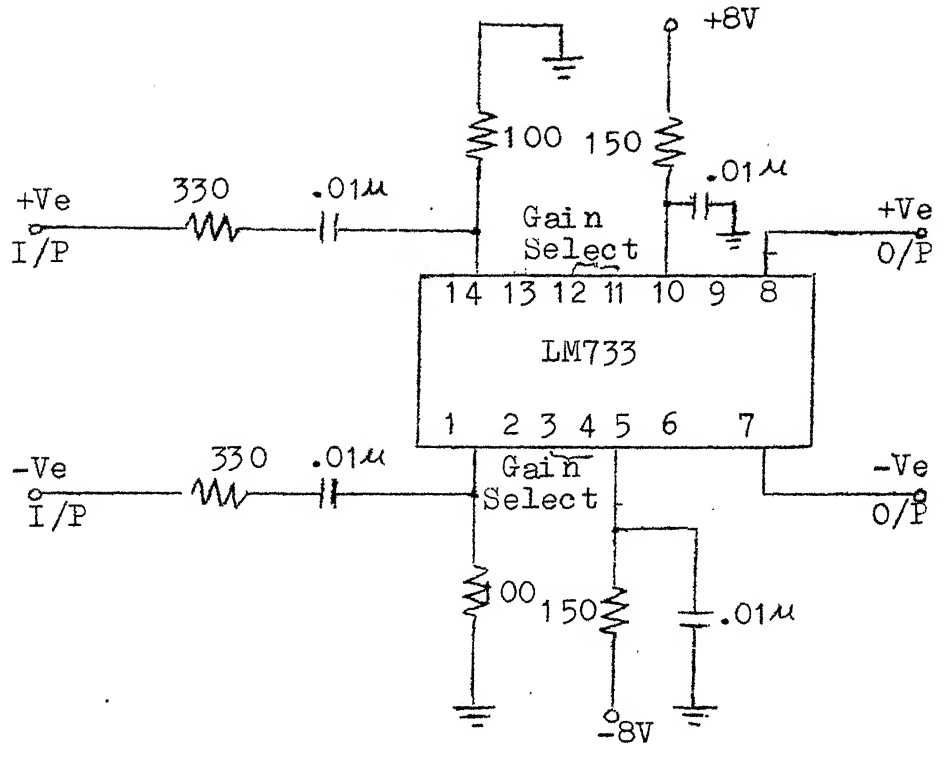


Fig. 3.6 Differential Amplifier

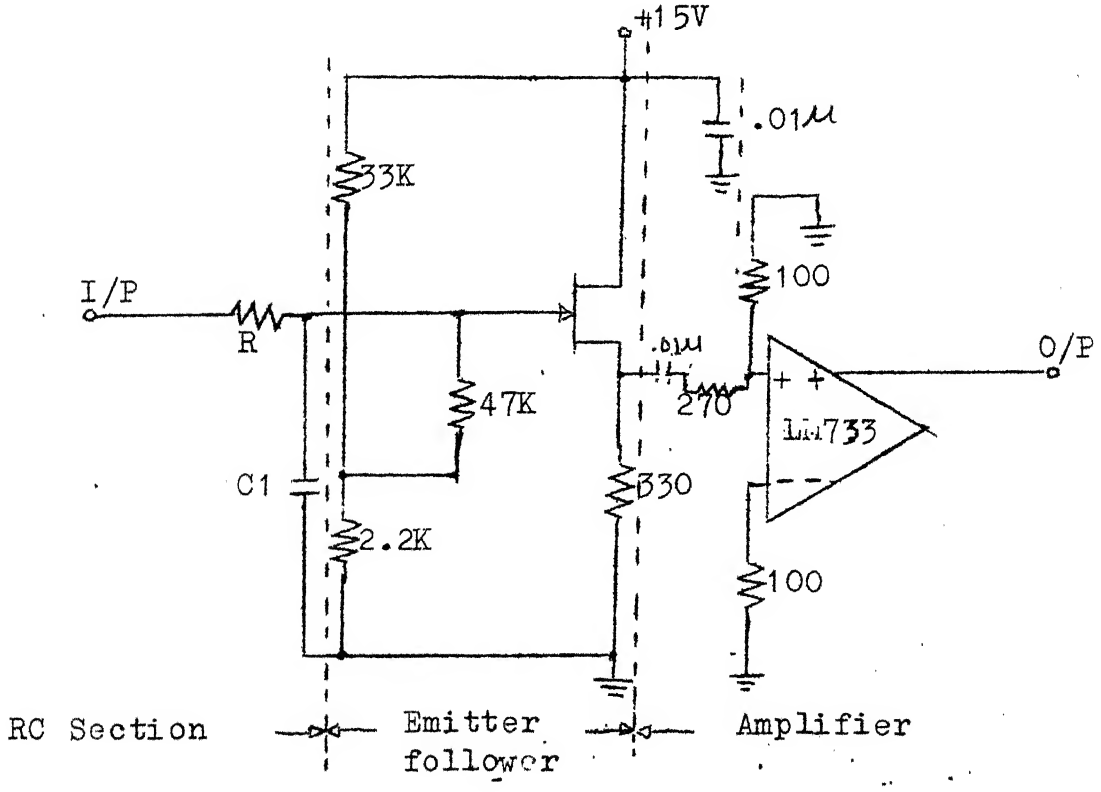


Fig. 3.7 Phase Shifter

3.2.6 Biphase Modulator

The biphase modulation (BPSK) is achieved by using balanced modulator LM1496. The biphase modulator is characterized as

When Modulating signal = +ve; Modulated signal = Carrier without any phase difference.

Modulating signal = -ve; Modulated signal = Carrier with 180° phase difference

The modulating signal amplitude is chosen to be $\pm$.5V because the modulator saturates at about $\pm$.15V. Thus the output is free from amplitude variations, whereas there are changes in phase. The circuit diagram of biphase modulator is given in Fig. 3.8. The differential output of the modulator is fed to a differential amplifier which provides the proper gain and also tries to nullify the carrier leakage.

3.2.7 Adder

The addition of the two biphase channels (P and Q) is performed by using the differential amplifier, LM733, (Fig. 3.9). The output of the adder is the required QPSK signal.

3.3 DESIGN OF DEMODULATOR

The received signal is fed to the demodulator with the objective to get the transmitted binary data as its output.

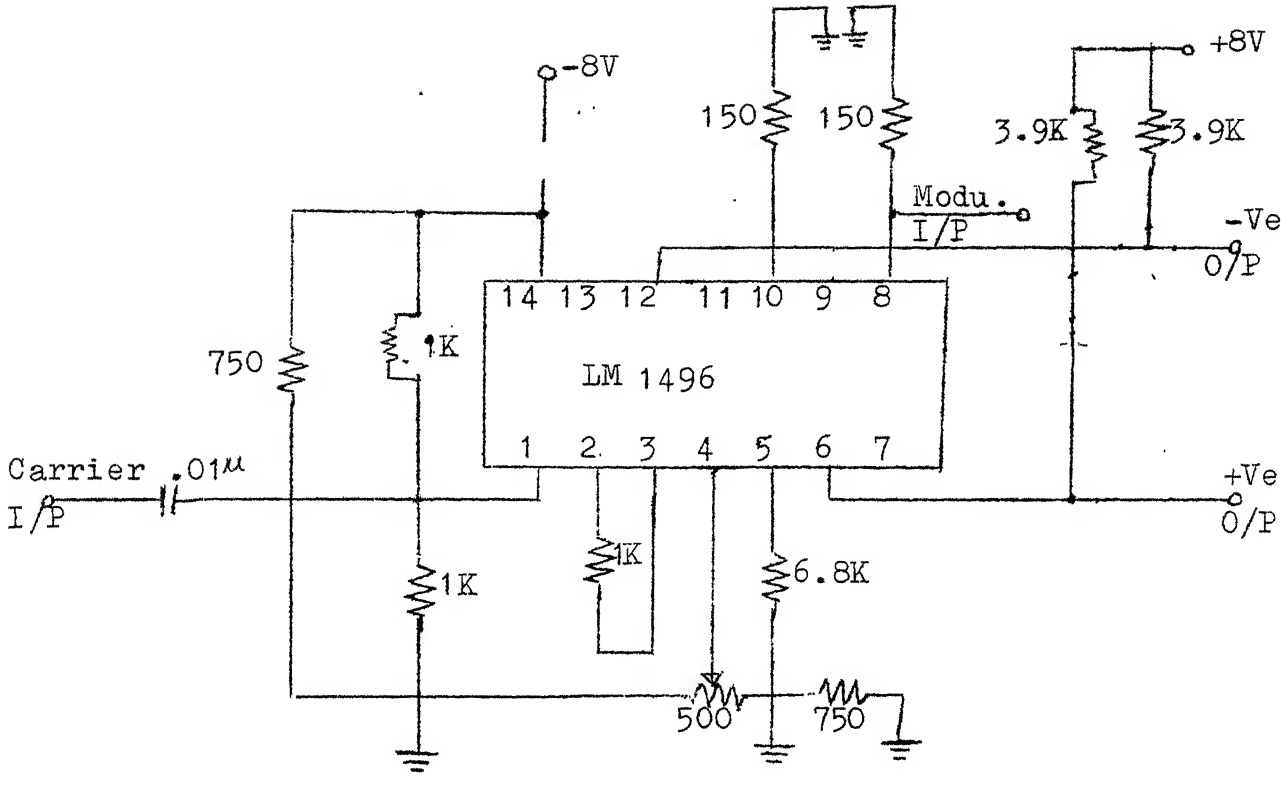


Fig. 3.8 Biphase Modulator

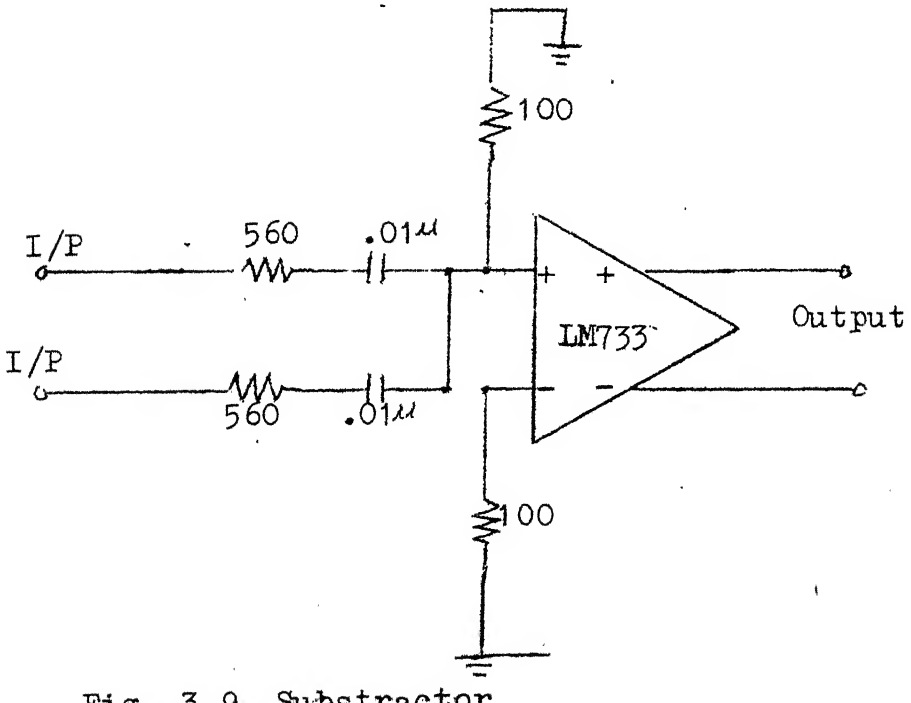


Fig. 3.9 Substractor

The objective is met with the help of a decision logic and processor circuitry which detects the transmitted data. To achieve this, the received signal is to be demodulated. Carrier recovery and clock recovery circuits are needed for unambiguous demodulation.

3.3.1 Carrier Recovery Circuit

It has been concluded in Sec. 2.3.1 that for QPSK the Costas loop is an optimum choice for carrier recovery. The Costas loop exhibits three equally probable ambiguities in the interval $(0, 2\pi)$. In our case the ambiguities are 90°, 180° or 270°. It implies that the recovered carrier may have a phase difference of 90° or 180° or 270° instead of having zero phase difference as required. Thus, if recovered carrier has any phase difference from fixed reference, the detected data should be corrected accordingly. This basically means a constant phase difference is to be introduced at all levels. This is done in the converter of the demodulator with the help of 4-line to 1-line data selector. Table 3.1 shows the relationship between different ambiguities and corresponding corrections to be made in detected data. The loop consists of phase detectors, multipliers, loop filter, voltage controlled oscillator (VCO) and phase shifters.

3.3.1.1 Phase Detector

A phase detector consists of a multiplier followed by

a low pass filter. The output of the phase detector is proportional to the cosine of phase difference between two input signals. The multiplier has been realized by LM 1496 whereas an RC section has been used for low pass filter. The differential output of the multiplier is fed to an operational amplifier (CA3100) through the low pass filters, which increases the signal level. The slew rate of the Op-Amp. is moderate, so it also suppresses some undesired higher frequencies. The complete circuit diagram of the phase detector is shown in Fig. 3.10. The following is the typical characteristic of the phase detector.

Phase detector sensitivity = 1.66 V/rad.

Cutoff frequency of LPF = 2.84 MHz

Though, the 3 dB frequency of the LPF is required to be only 1.25 MHz, wider bandwidth (2.84 MHz) of LPF gives less distorted output waveforms and simultaneously the attenuation of higher frequency (20 MHz) will not be much degraded.

3.3.1.2 Multiplier

The only difference in the multiplier and phase detector (as discussed above) is that in multiplier there is no low pass filter. The differential output of the multiplier LM1496 is directly connected to the differential input of differential amplifier CA 3100 without any RC section (LPF) in between. All other values of components used are the same as in the phase detector.

TABLE 3.1

Relationship between ambiguity and corresponding correction

Phase of recovered carrier with respect to correct reference	Transmitted dibit		Detected dibit		Correction to be made to get correct dibit		State of select switch for correcti	
	d_1	d_2	q_1'	q_2'	q_1	q_2	A	B
0°	D_1	D_2	D_1	D_2	q_1'	q_2'	0	0
90°	D_1	D_2	$\bar{D}_2$	D_1	q_2	$\bar{q}_1$	1	0
180°	D_1	D_2	$\bar{D}_1$	$\bar{D}_2$	$\bar{q}_1'$	$\bar{q}_2'$	0	1
270°	D_1	D_2	D_2	$\bar{D}_1$	$\bar{q}_2'$	q_1'	1	1

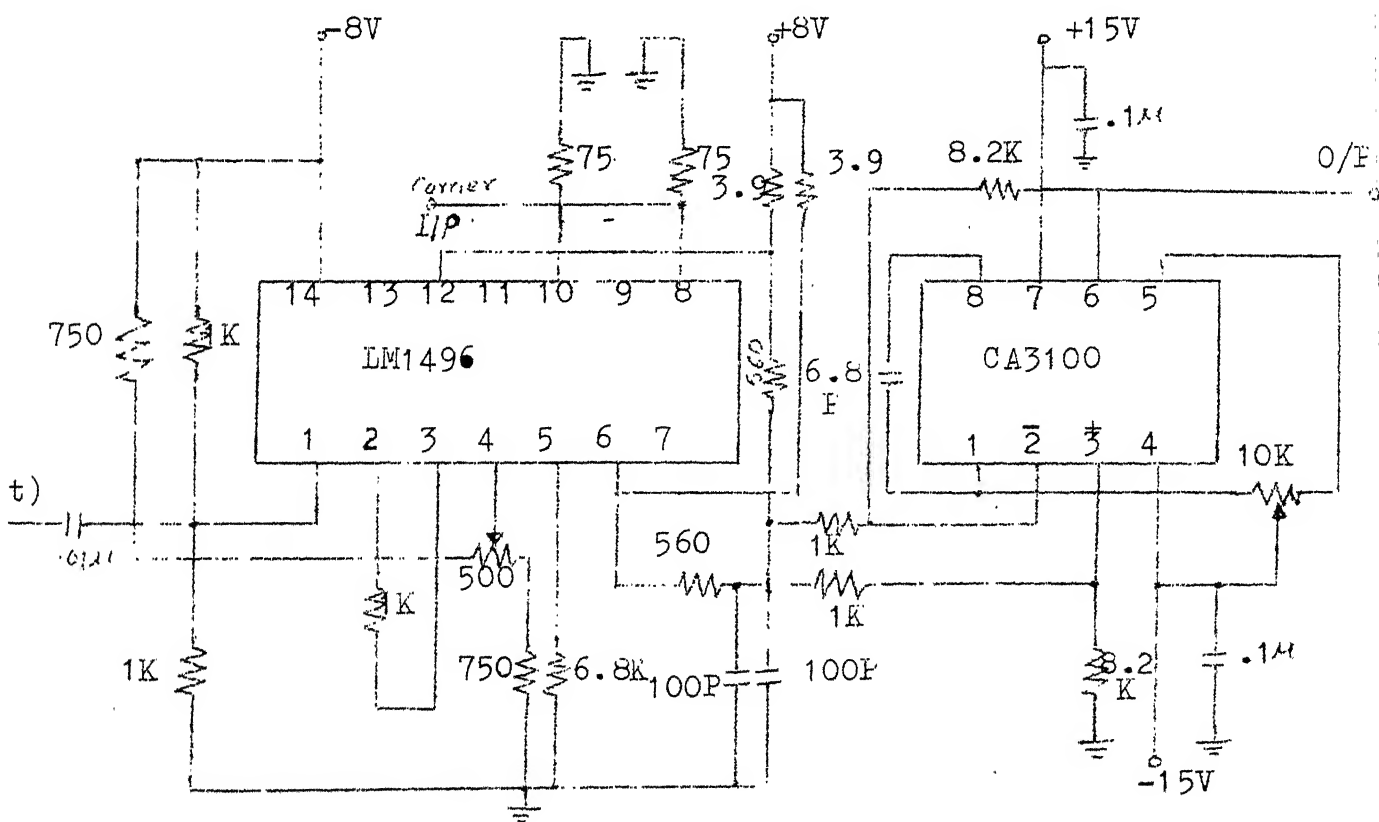


Fig. 3.10 Phase Detector.

3.3.1.3 Loop Filter [3,21]

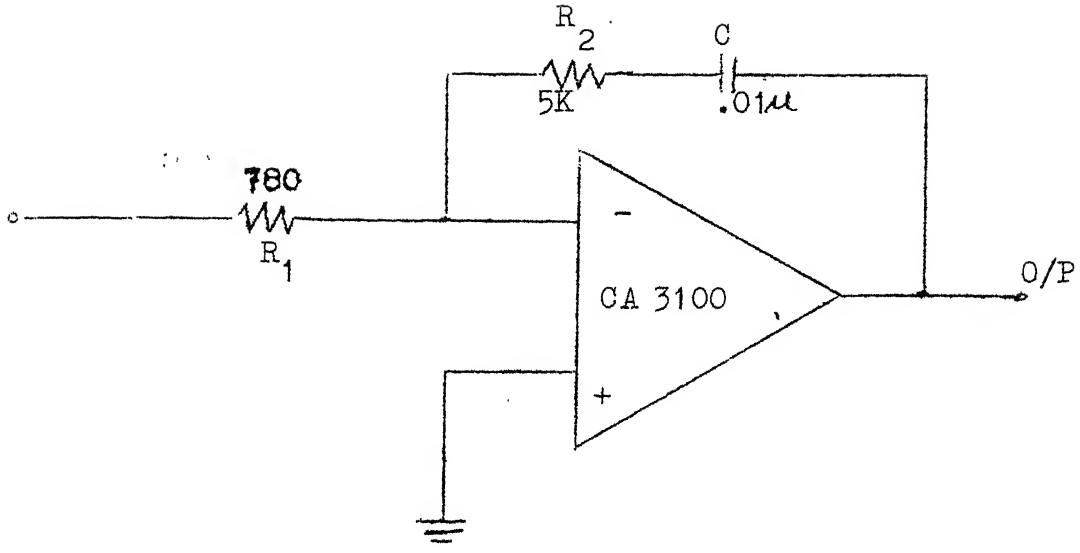
Loop filter is low pass filter that is placed between the phase detector output and the VCO modulation input. Fundamental loop characteristics such as capture range, loop bandwidth, capture time, and transient response are controlled primarily by the loop filter. The study of the phase-locked loop response to various disturbances reveals that the performance of the first order loop is not particularly outstanding. It is consequently necessary, in many cases, to increase the order by inserting a loop filter in the loop. The most frequently used devices are discussed in [21] . Finally, the integrator, with phase lead correction network, the transfer function (K_F) of which is given by Eqn. (3.2) is chosen. The circuit diagram of the loop filter is shown in Fig. 3.11(a)

$$K_F = \frac{1 + T_1 s}{T_2 s} \qquad (3.2)$$

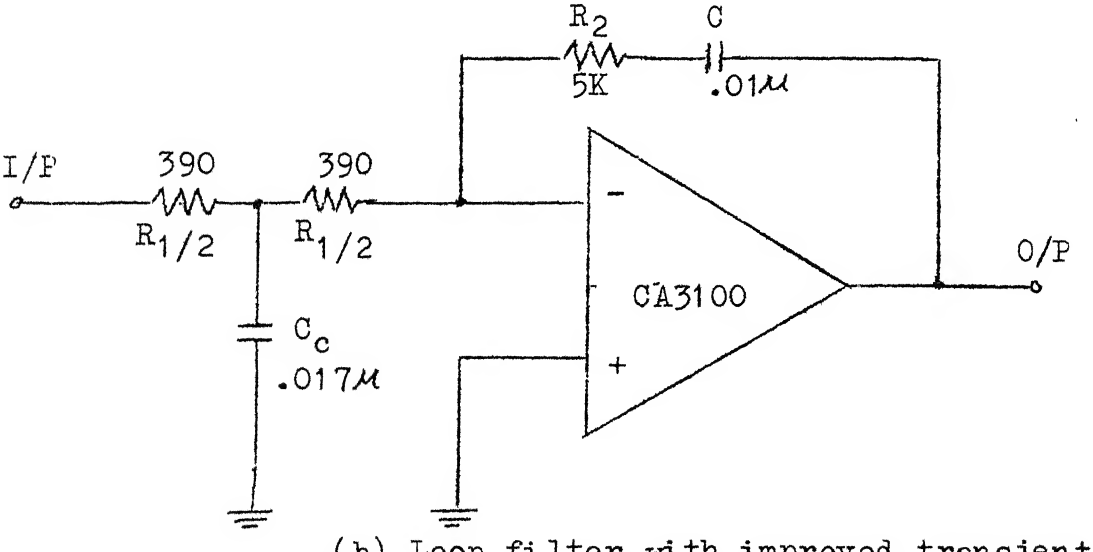
where $T_1 = R_2 C$

$T_2 = R_1 C$

To make transient suppression independent of amplifier response, the network may be embedded within the input resistor R_1 (Fig. 3.11(b)). Besides rounding off/inhibiting and pulses, this network adds an additional pole to the loop and may cause further overshoot, if the cutoff frequency (w_c) is too close to the natural frequency (w_n) of loop. It is desirable to have w_c five to ten times w_n to get rid of this



(a) Loop Filter



(b) Loop filter with improved transient suppression.

Fig. 3.11 Loop Filter.

problem. With these considerations, our system has the following specification.

Lock-up time = 140 μ sec

w_n = 31K rad/sec.

Damping ratio ξ = .8

Lock range = $\pm$ 1.25 KHz around centre frequency (10 MHz)

Capture range = $\pm$ 1.0 KHz around centre frequency (10 MHz)

$$w_c = 8\, w_n$$

where $$w_c = \frac{4}{R_1 C_c}$$

3.3.1.4 Voltage Controlled Oscillator

Since the carrier frequency is very stable at the receiver (in Costas loop), the required frequency variation in voltage controlled oscillator, which tracks the carrier, is very small. We have designed voltage controlled crystal oscillator (VCXO) because of this small frequency variation. The centre frequency (when control voltage V_c is zero) is 10 MHz The frequency variation is not very linear because of non-linear behaviour of the varactor diode. The control voltage may vary between +14V to -14V. The VCXO frequency decreases when control signal is positive and vice-versa. The complete circuit diagram is shown in Fig. 3.12. Some adjustment of C_1 is necessary to put the crystal at exact centre frequency, i.e.,

10 MHz. The VCXO is followed by an emitter follower to avoid the loading. The output level of VCXO is observed to be around 1.0V peak-to-peak.

3.3.2 Clock Recovery

The baseband rectifiers have been used for clock recovery. The detected signals of both channels P and Q (Fig. 3.2) are fed to the clock recovery circuit. The theoretical details have already been discussed in Sec. 2.3.2. It is assumed that the data varies randomly. A long stream of 1s or 0s are not allowed because clock recovery is not feasible with such long sequences of either a 0 or a 1. Now we shall consider the realization of the complete clock recovery circuit.

3.3.2.1 Rectifier

A full wave rectifier has been used (Fig. 3.13). Since the signal frequency is high with small amplitude, the point contact diodes (0A81) have been used for rectification. Since, the input of the rectifier is bipolar signal, the frequency of output will be double of the input frequency.

3.3.2.2 Differential Amplifier

The output of rectifier is amplified by using a differential amplifier. The required amplifier is realized by using an OP-AMP, CA 3100, having a moderate slew rate.

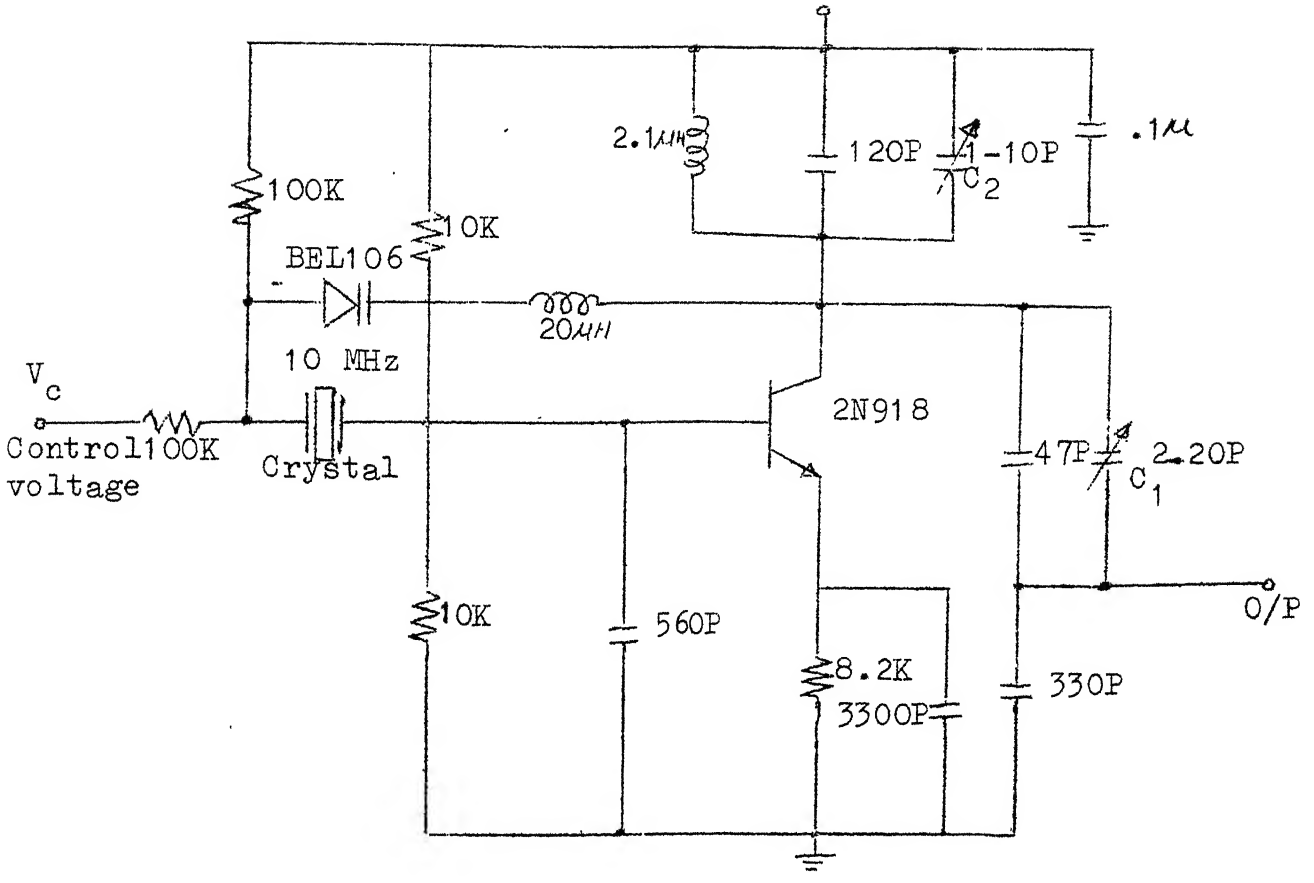


Fig. 3.12 Voltage controlled crystal oscillator (VCXO)

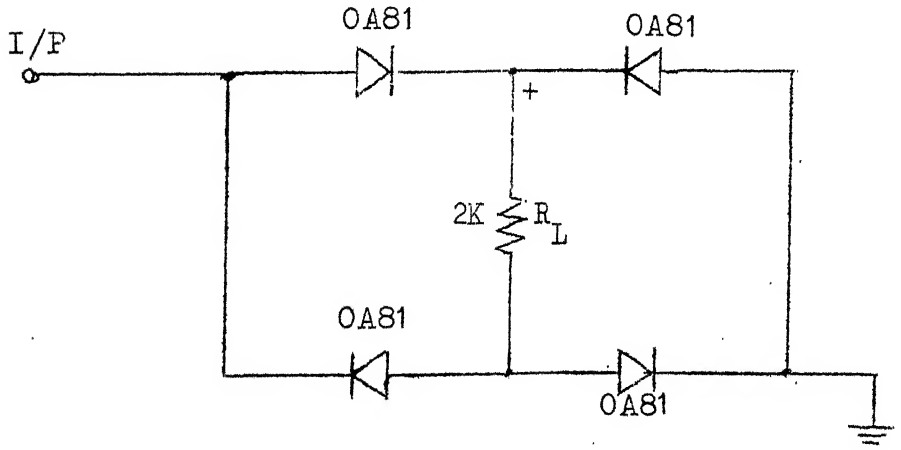


Fig. 3.13 Full wave rectifier.

The configuration shown in Fig. 3.14 is used. The gain of the amplifier is given by

$$\text{Gain} = \frac{R_2}{R_1}$$

3.3.2.3 Adder

The addition of two channels is performed by the OP-AM (CA 3100). Since one channel gets inverted, what we really need is a substracter instead of adder. Thus the same configuration as discussed above (Fig. 3.14) (with gain = 1) is used.

3.3.2.4 Clock Filter

The clock filter design is shown in Fig. 3.15. The tank circuit is tuned to the frequency $\frac{f_s}{2}$, i.e. 1.25 MHz. At this place, a class C tuned amplifier could also be used. The filter is followed by an emitter follower to avoid the loading. The value of C used differs from calculated value because of input capacitance of emitter follower.

3.3.2.5 Phase-Locked Loop (PLL)

The clock filter which has been used is a single tuned filter. So to avoid the cycle skips a phase-locked loop (PLL) has been employed which tracks the input frequency. The frequency of the output of the clock filter is $\frac{f_s}{2}$ whereas actual clock frequency is f_s. So with the help of the PLL

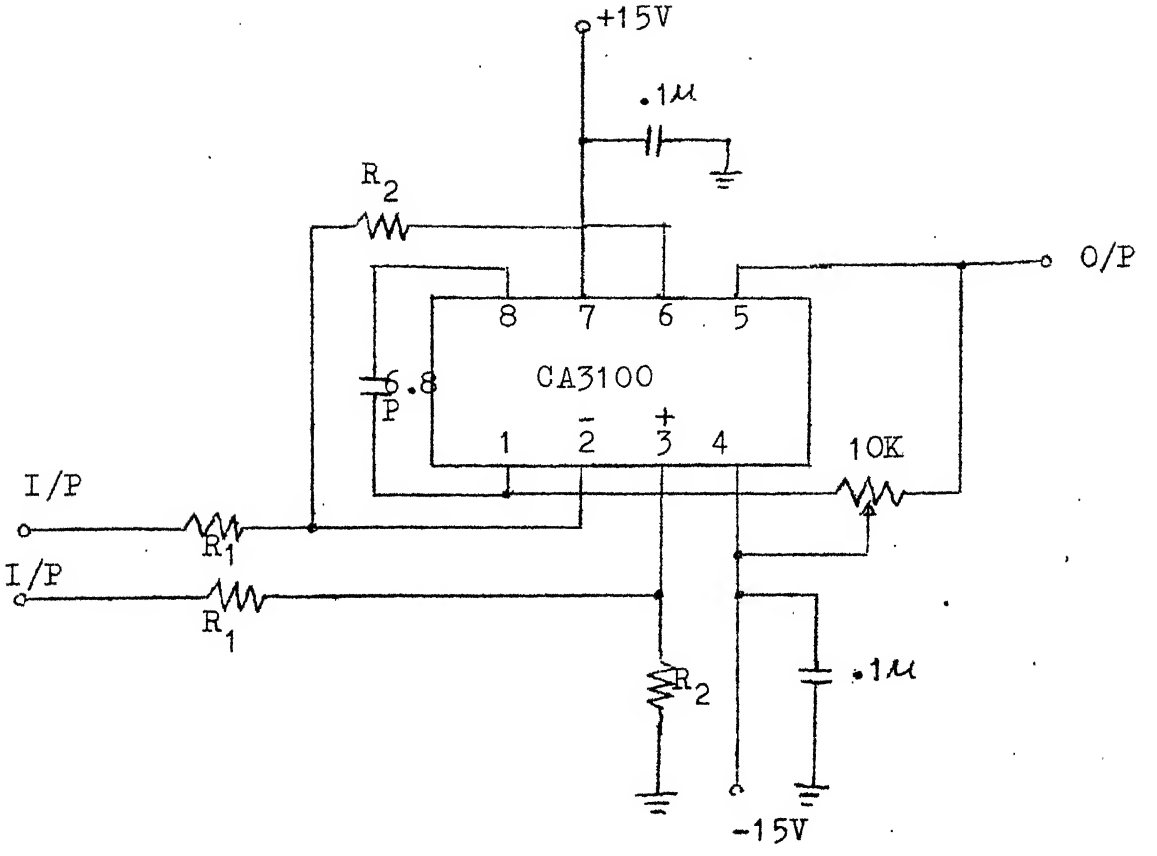


Fig. 3.14 Differential Amplifier

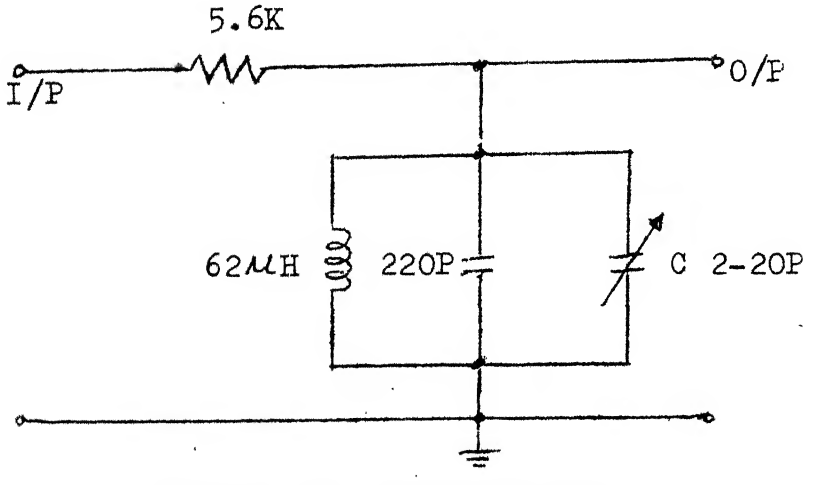


Fig. 3.15 Clock Filter

and a divide-by-two circuit, the required frequency (2.5 MHz) is synthesized. The required characteristics of the PLL is that once it is locked, it should not be unlocked immediately. This implies that PLL should take a long time to be completely unlocked. For example, with the PLL in lock, if a stream of 1s or 0s is received, the output frequency of the clock filter changes. Since our requirement is that our recovered clock should not loose the synchronization, the PLL must take more time to be unlocked. During this time the stream of 1's or 0's would be over and thus correct reference can be maintained. However a very long stream of 1's or 0's will cause the synchronization to be lost. The XR-215 have been used for synthesis of PLL with following parameters (Fig. 3.16).

Centre frequency = 2.5 MHz
Lock range = 409.5 KHz
Capture range = 22.1 KHz

3.3.2.6 Comparator

The comparator is used to make the signal TTL compatible. The positive voltage corresponds to 1. For this purpose, μA 710 has been used as shown in Fig. 3.17. The comparator can drive only one TTL input.

3.3.2.7 Divide-by-two

The divide-by-two function is performed by using D-type

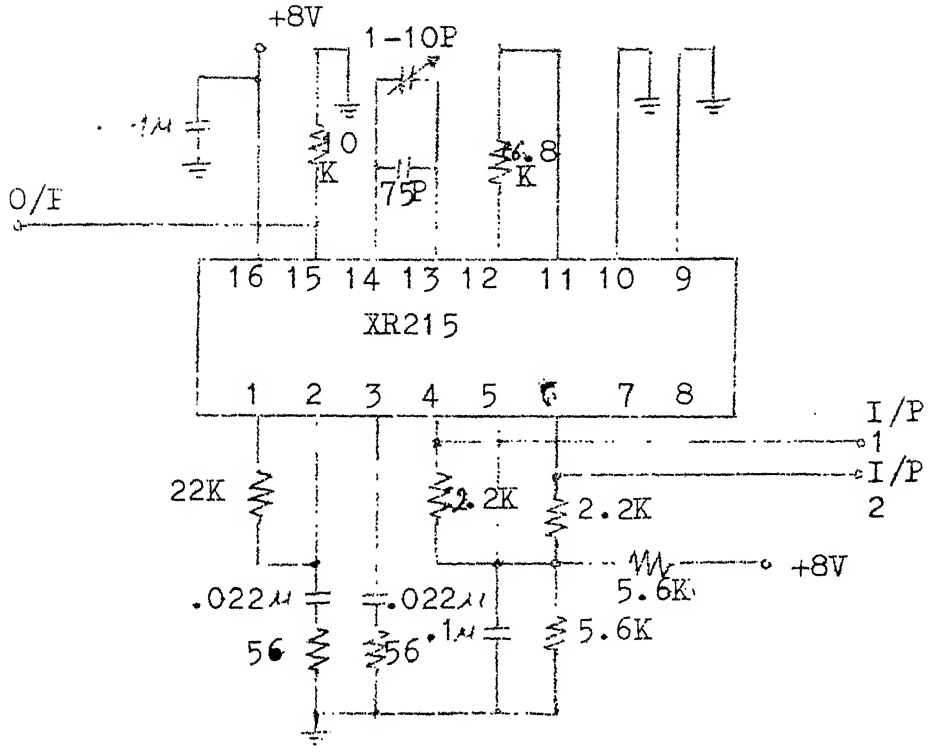


Fig. 3.16 Phase-locked loop (PLL)

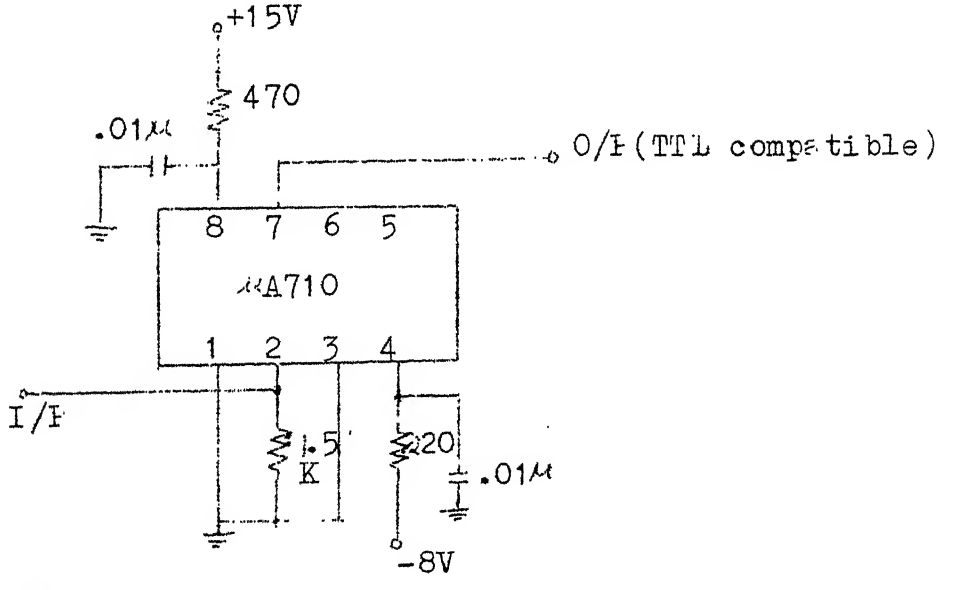


Fig. 3.17 Comparator

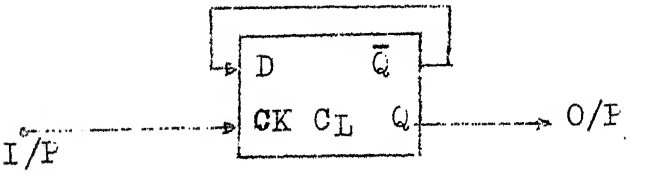


Fig. 3.18 Divide-by-Two

flip-flop (SN 7474). The circuit diagram is shown in Fig. 3.18. The flip-flops are to be cleared before the operation starts.

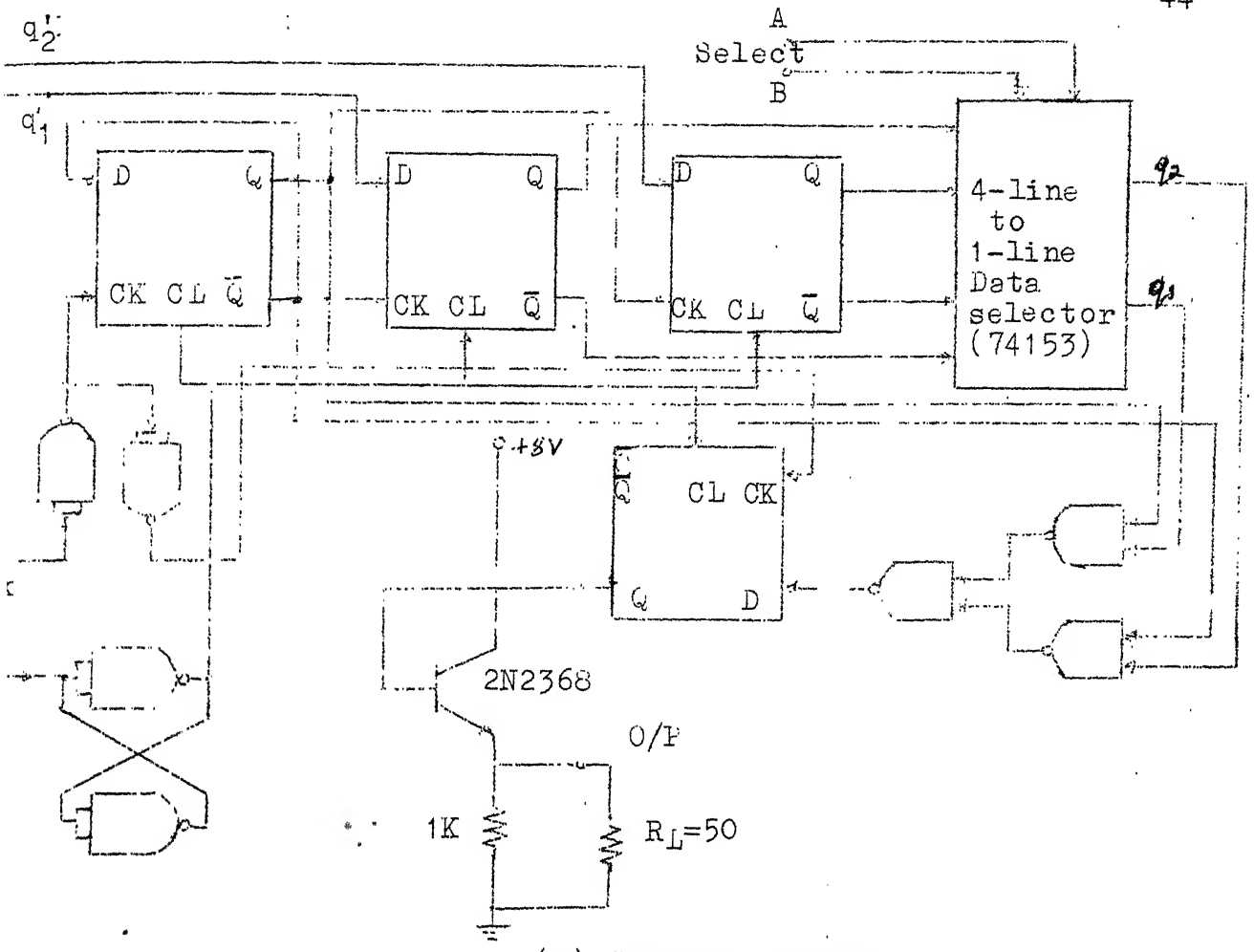
3.3.3 Decision Logic and Processor

Firstly, the signals $q_1(t)$ and $q_2(t)$ of both the channels are made TTL compatible by the comparator. The comparator has the same configuration as discussed in Section 3.3.2.6.

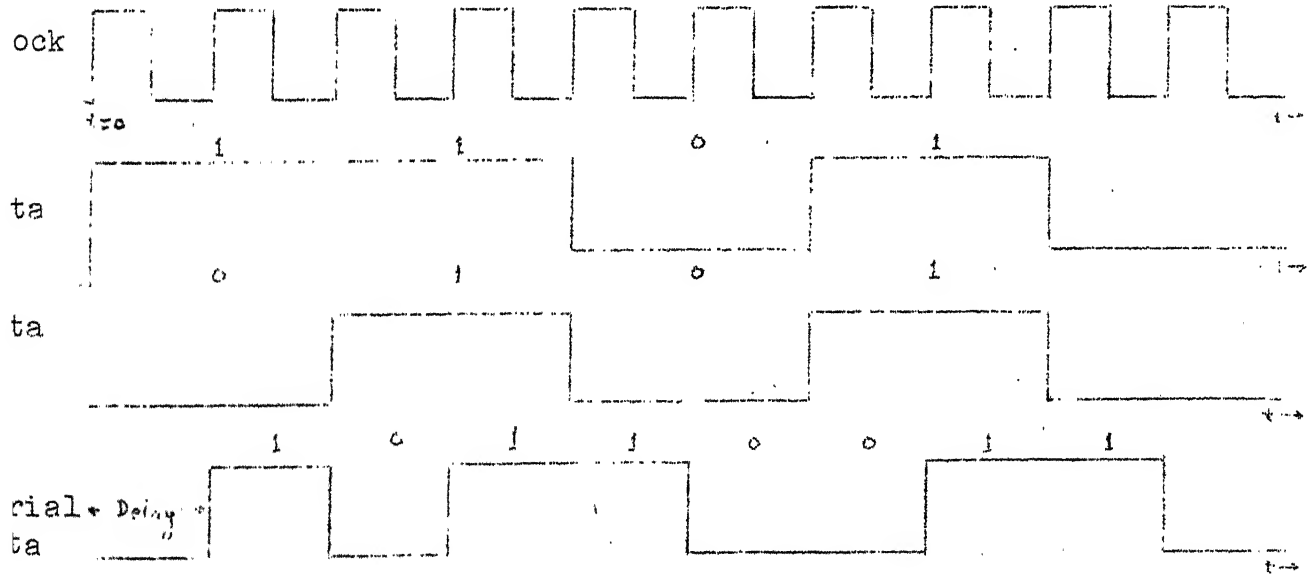
If there is no error, q_1 and q_2 will correspond to d_1 and d_2 respectively. Here the inverse of the operation (as carried out at the modulator) has to be performed to receive the serial data. The theoretical description is given in Section 2.3.3. The complete circuit diagram is shown in Fig. 3.19 with input and output waveforms. The 4-line to 1-line data selector (SN 74153) has been used to resolve the ambiguity in Costas loop as discussed in Section 3.3.1. The relationship between phases and the state of select input is given in Table 3.1. An emitter follower has been used to avoid the loading which provides the demodulated output.

3.4 SIMULATION OF CHANNEL

Since it was not possible to test the modem on an actual physical channel, an ideal channel has been simulated. Gaussian noise is added to the modulated signal. The signal corrupted by noise is passed through a band pass filter (BPF).



(a) Circuit Diagram



(b) Input and Output Waveforms

Fig. 3.19 Decision logic and processor

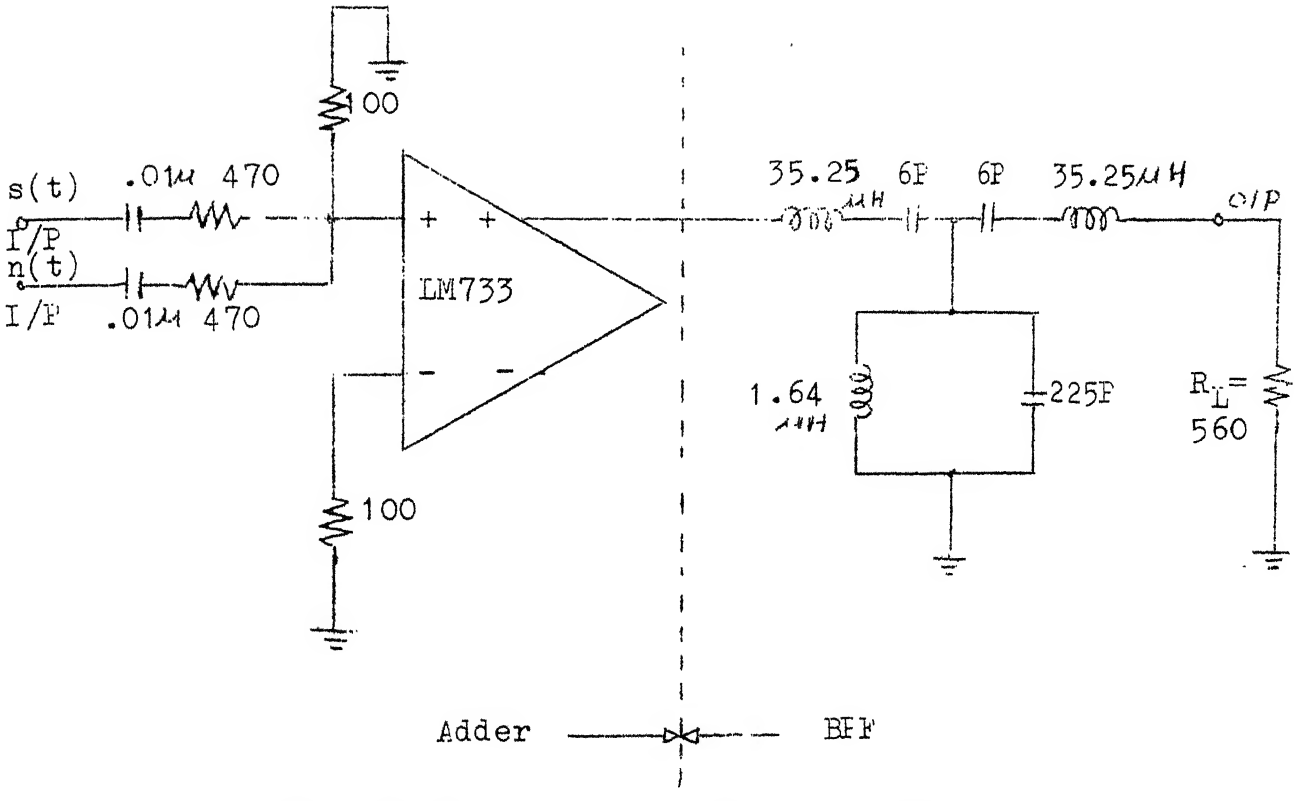


Fig. 3.20. Simulation of the Channel

The output of the band-pass filter is fed to the demodulator. The bandpass filter has the following characteristics (Fig. 3.2

Characteristic resistance	=	560Ω
Centre frequency	=	10 MHz
Upper cutoff frequency	=	11.34 MHz
Lower cutoff frequency	=	8.81 MHz

The QPSK signal has a bandwidth of 1.25 MHz hence the bandpass filter should also have the same bandwidth. But due to nonavailability of the proper components, such a sharp BPF was not possible. The noise has been generated by a random noise generator (Type 1390-B, serial 6389, G.R.C., U.S.A.)

3.5 DISCUSSION

The complete circuit diagram of the modulator and the demodulator has been appended at the end of this thesis. The used values of the components differ slightly from the corresponding calculated values due to the tolerance of the component availability.

CHAPTER 4

PERFORMANCE OF THE MODEM

The fabricated modem has been tested in the laboratory environment. The performance of the modem is studied when the channel is assumed to be an AWGN channel. We assume that there is no intersymbol interference (ISI) and the delay distortion is negligible. The modulated signal is corrupted by adding noise from a noise generator. This corrupted signal is fed to the demodulator and the performance is evaluated. The data to be transmitted is obtained from a data generator and the detected data is fed to an error detector. Thus for different values of bit SNR the corresponding bit error rates (BER) are obtained experimentally. The bit error rate (BER) corresponding to each value of bit SNR is also computed. The experimental and theoretical results (Table 4.1) are plotted in Fig. 4.1.

The overall experimental setup for measurement purposes has been shown (in the block diagram form) in Fig. 4.2. Various pin connections are also available for seeing waveforms on a CRO at various stages of the progress of a data stream from the source to the sink. For SNR measurement (at the input of the receiver), we have used an r.m.s. voltmeter. Firstly, the signal without noise is measured (say it is E_o). Then we add

TABLE 4.1

Probability of Error for QPSK Modem

Bit SNR dB E_b	Theoretically obtained BER	Experimentally obtained BER
0.6534	6.17×10^{-2}	9.3×10^{-2}
2.2915	3.23×10^{-2}	4.5×10^{-2}
4.9557	6.16×10^{-3}	1.1×10^{-2}
5.4130	4.17×10^{-3}	7.5×10^{-3}
6.4067	1.56×10^{-3}	3.0×10^{-3}
6.9498	8.26×10^{-3}	1.8×10^{-3}
7.8338	2.46×10^{-4}	5.4×10^{-4}
8.8182	4.61×10^{-5}	1.2×10^{-4}
9.5424	1.11×10^{-5}	2.7×10^{-5}
9.9285	4.6×10^{-6}	1.1×10^{-5}
10.3326	1.75×10^{-6}	2.2×10^{-6}

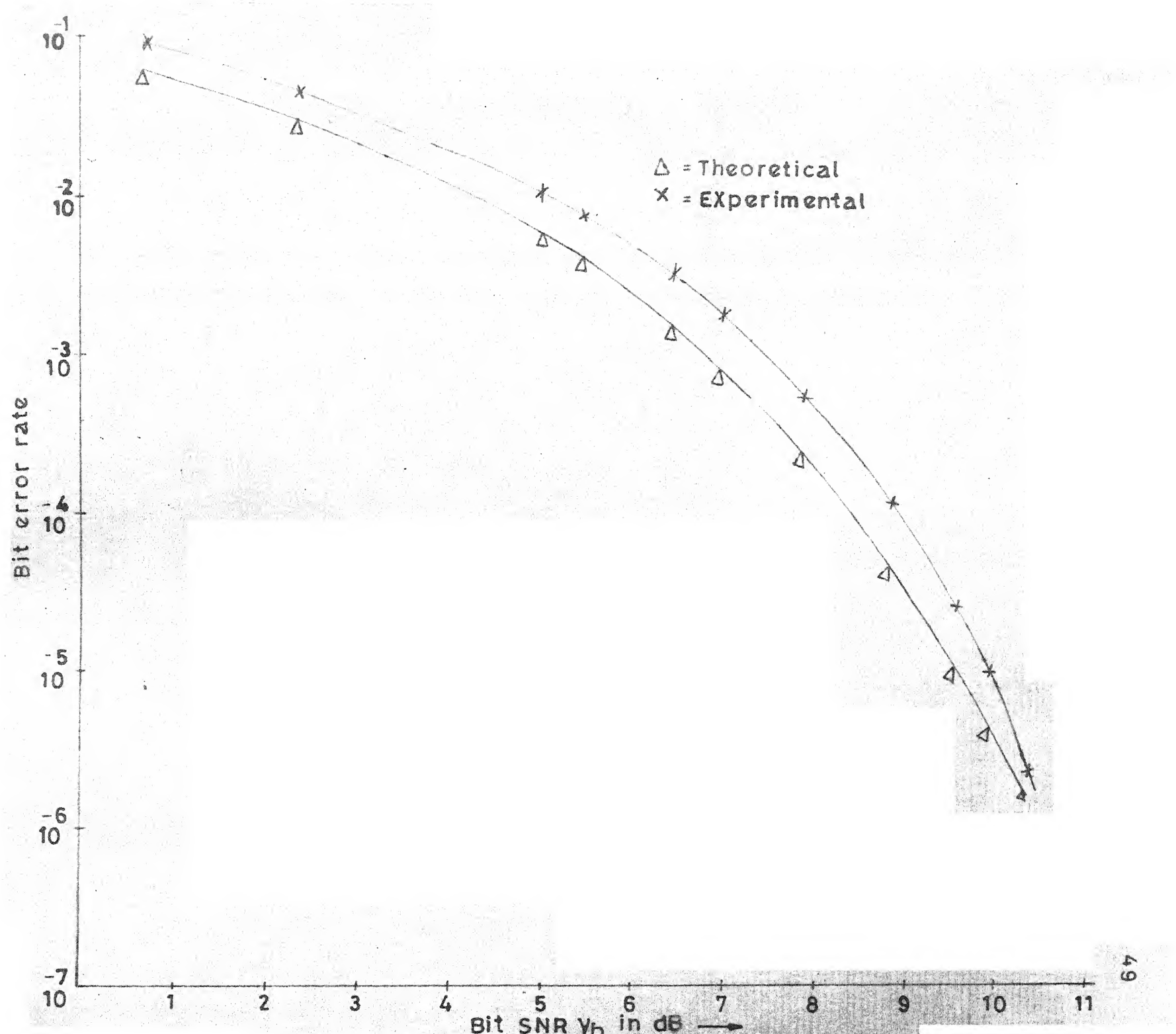


Fig. 4.1 Bit SNR Vs Bit error rate

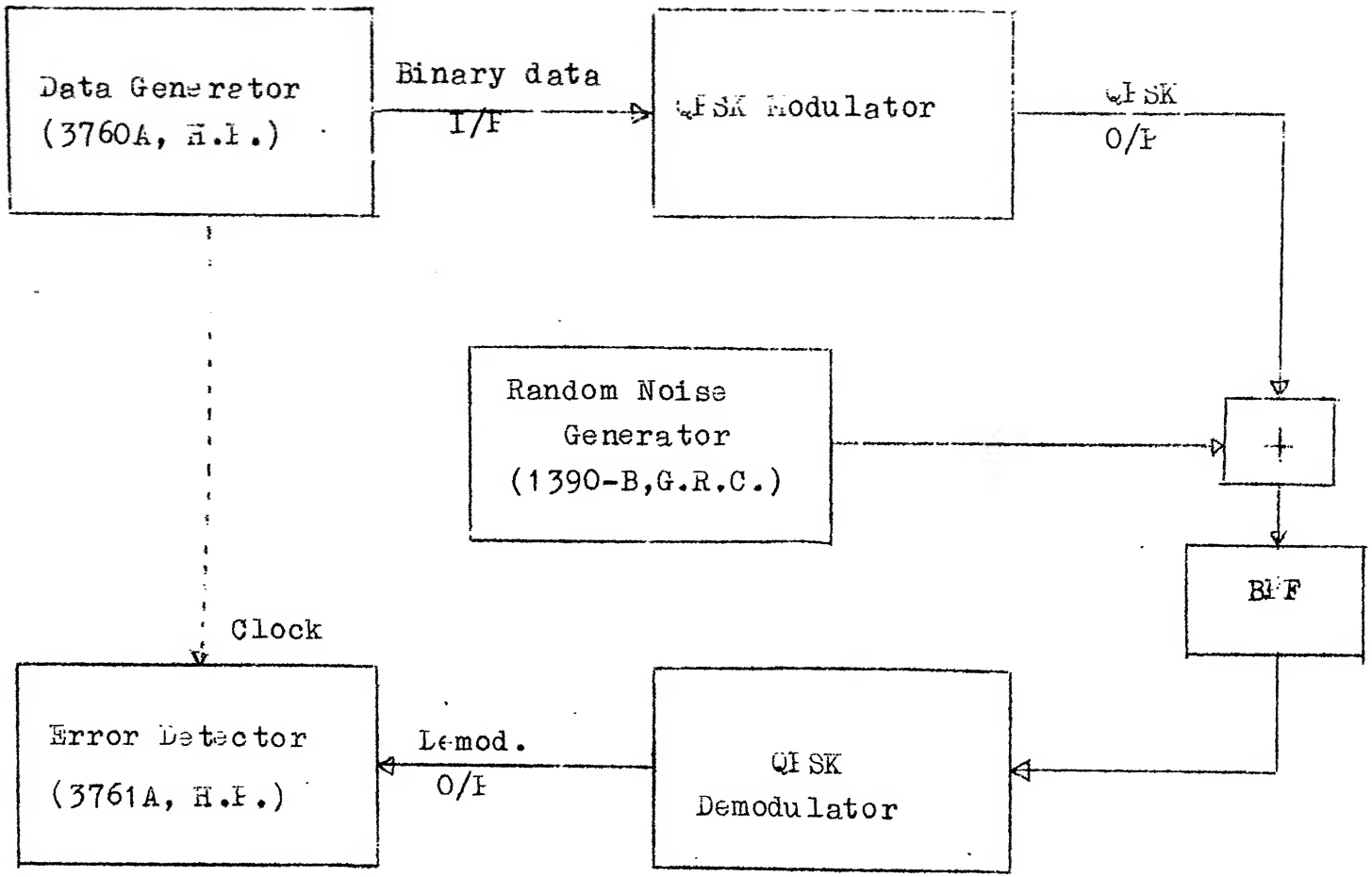


Fig. 4.2 Evaluation of the System Performance

noise in the signal and the corresponding resultant signal is measured (say it is V_o). Thus SNR becomes

$$SNR = \frac{E_o^2}{(V_o - E_o)^2}$$

$$= 20 \log \frac{E_o}{V_o - E_o} \text{ dB} \qquad (4.1)$$

It is seen from Fig. 4.1 that experimental bit SNR for the modem differs from computed value by a maximum of 0.7 dB which occurs at approximately 10^{-3} BER. Also, for bit SNR of more than 9.0 dB, the experimental results coincide closely to its theoretical value. The difference in bit SNR is due to the hardware implementation.

The QPSK signal has a bandwidth of 1.25 MHz but we have used a bandpass filter of 2.53 MHz bandwidth. So the noise associated with the signal will be more which will degrade the performance of the modem. We tried to keep the centre frequency of voltage controlled crystal oscillator (in carrier recovery circuit) equal to the carrier frequency but the two frequencies could not be made exactly equal resulting in noisy recovered carrier. This may be another reason for further degradation of the performance. The phase jitters also result in poor performance. We have demonstrated that the practical system works within 0.7 dB of the theoretical model.

CHAPTER 5

CONCLUSION

A communication engineer's dream is to design an efficient modem to accomodate as large a number of channels as possible at as high a data rate as possible (at an acceptable fidelity criterion). An attempt has been made in this direction by using the modulation techniques which provide a very good data rate per unit bandwidth (R/B) performance. A typical secondary objective is to achieve this bandwidth efficiency at a minimum practical expenditure of average signal-to-noise ratio in an additive white Gaussian noise channel. Though the M-ary PSK provides a very good R/B performance, it is one of the most complex systems for practical implementation. As a compromise between the performance and the complexity of the system, QPSK system gives a good R/B performance. Hence this study has been carried out. We have shown in Chapter 4, that the performance of the fabricated QPSK modem in an AWGN channel is quite satisfactory.

The subcarrier frequency is quite high so one has to be careful about the layout of the modem. The system requires very accurate and stable phase shift at various stages. In the fabrication process, because of the nonavailability of

high slew rate operational amplifiers we could not realize the phase shifters with ease. Since the frequency is quite high a small stray capacitance can give a good amount of error in the phase. Though the phase shifters (used in modem) work well, the use of operational amplifiers will certainly improve the performance and the components needed will be very much reduced. The differential amplifier LM 733 has got a high gain and wide bandwidth. So it was giving trouble because of self oscillations. One must take care of its proper input and output terminations. In the phase detector, the offset null is very critical. The correct centre frequency of the voltage controlled crystal oscillator is obtained by adding an inductance in series with the crystal. Though, we have tried our best to keep the centre frequency of VCXO and carrier frequency exactly the same, slight difference could not be completely eliminated resulting in a very small phase error in carrier reference. The carrier recovery can also be obtained by baseband analog or digital processing. In case of baseband digital processing, the carrier recovery circuit can be composed of a very small number of components. We have used a passive clock filter. An active filter (notch filter) would have further improved the performance of clock recovery circuit. A cost analysis of the modem is given in Appendix I.

The modem works well at 2.5 Mbps. However, one would like to design a modem at higher data rate. This could be achieved by using high subcarrier frequency and correspondingly appropriate components. Also the phase ambiguity of the recovered carrier could be resolved by using suitable coding/decoding schemes. Here we have not considered the effect of intersymbol interference, delay distortion and phase jitters. Phase jitters are very destructive for this type of system. One can also go for 8Ø PSK for better R/B performance provided the components are available.

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APPENDIX I

CARD DESCRIPTION

The modem consists of three cards (PCB)

Card No.	Details	No. of ICs used
1	Modulator	12
2	Demodulator I	20 (from IC1 to IC20)
3	Demodulator II	12 (from IC21 to IC32)

The pin connections of the cards are shown in Fig. I.1.

POWER SUPPLY

The modem requires +5VDC, ±8VDC and ±15VDC voltages for its operation. We provide the required d.c. voltages from external sources.

TIME LAG

The time lag between input and output of the modem is 1.54 μsec.

COST

The costs of the components used in modulator and demodulator are Rs. 650/- and Rs. 2250/- respectively. Keeping a rule of thumb for the production cost to be approximately 5 times the component cost, the cost of the modem would come approximately to Rs. 15000/-.

Card No. 1

1	NC
2	Modulated O/P
3	-8VDC
4	d''_2
5	CLR
6	Clock I/P
7	+5VDC
8	Data I/P
9	d''_1
10	+8VDC
11	+15VDC
12	GND

Card No. 2

1	+15VDC
2	-15VDC
3	Demodulated O/P 2
4	Demodulated O/P 1
5	NC
6	NC
7	NC
8	Modulated I/P
9	-8VDC
10	+8VDC
11	NC
12	GND

Card No. 3

1	GND
2	+8VDC
3	+15VDC
4	-15VDC
5	Demodulated I/P1
6	Demodulated I/P2
7	-8VDC
8	+5VDC
9	Data O/P
10	SELECT B
11	SELECT A
12	CLR

*NC $\Rightarrow$ Not connected

Fig. I.1 Pin Connections of the Cards.

APPENDIX II

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